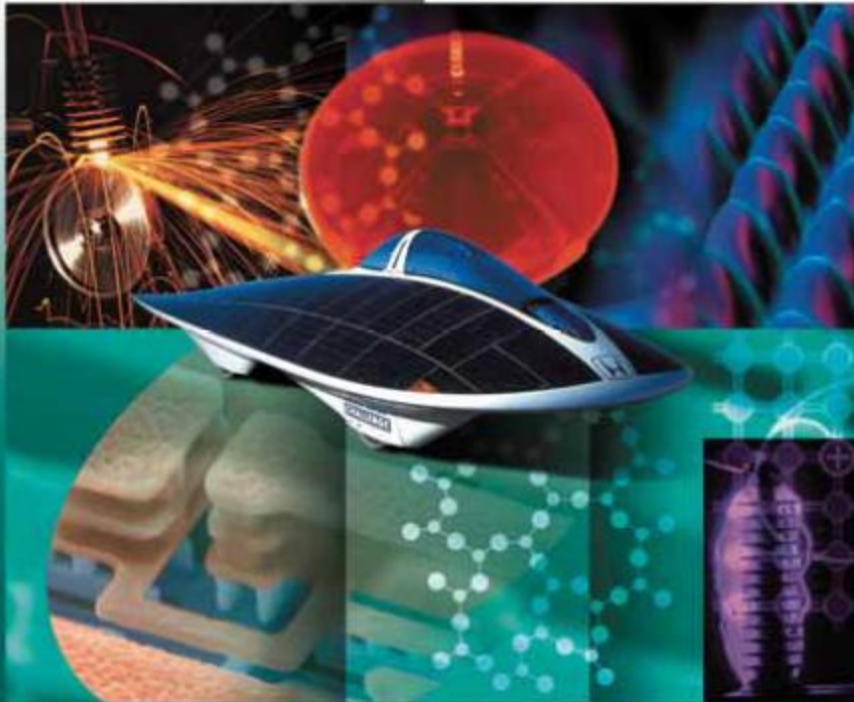


# Principles of Electronic Materials and Devices

Third Edition



S. O. Kasap

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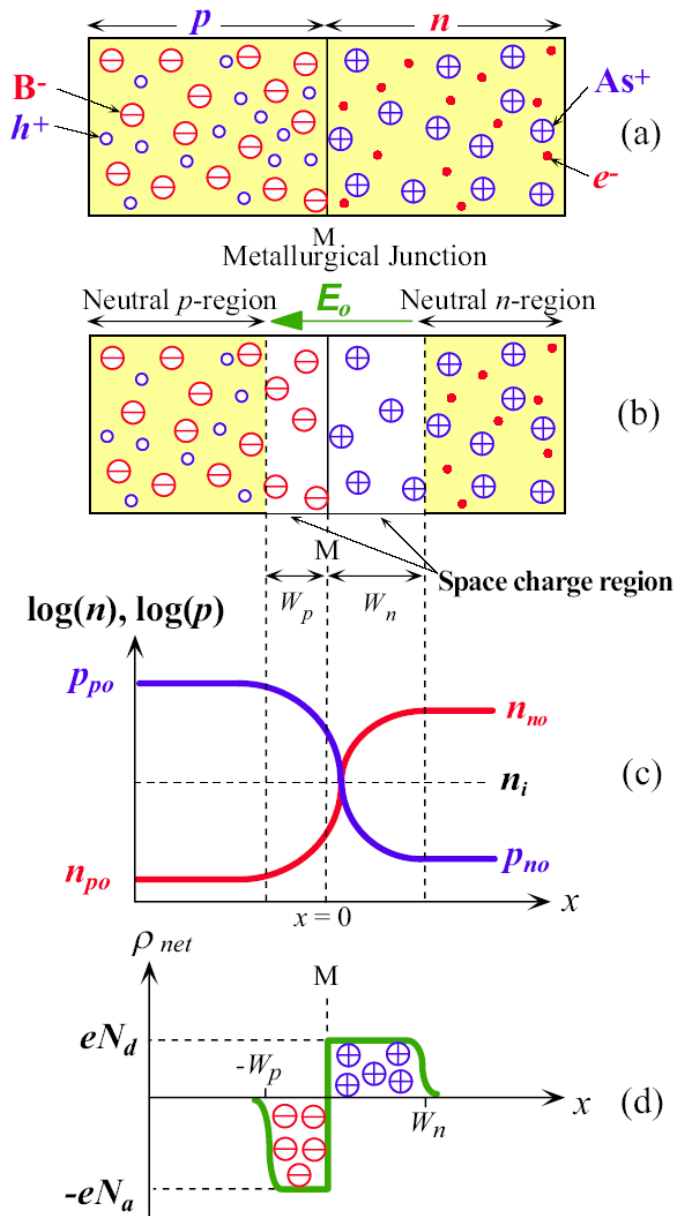
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***pn* Junction Si solar cells at work. Honda's two seated Dream car is powered by photovoltaics. The Honda Dream was first to finish 3,010 km in four days in the 1996 World Solar Challenge.**

**|SOURCE: Courtesy of Centre for Photovoltaic Engineering, University of New South Wales, Sydney, Australia.**

*From Principles of Electronic Materials and Devices, Third Edition, S.O. Kasap (© McGraw-Hill, 2005)*



## Properties of the pn junction

Fig 6.1

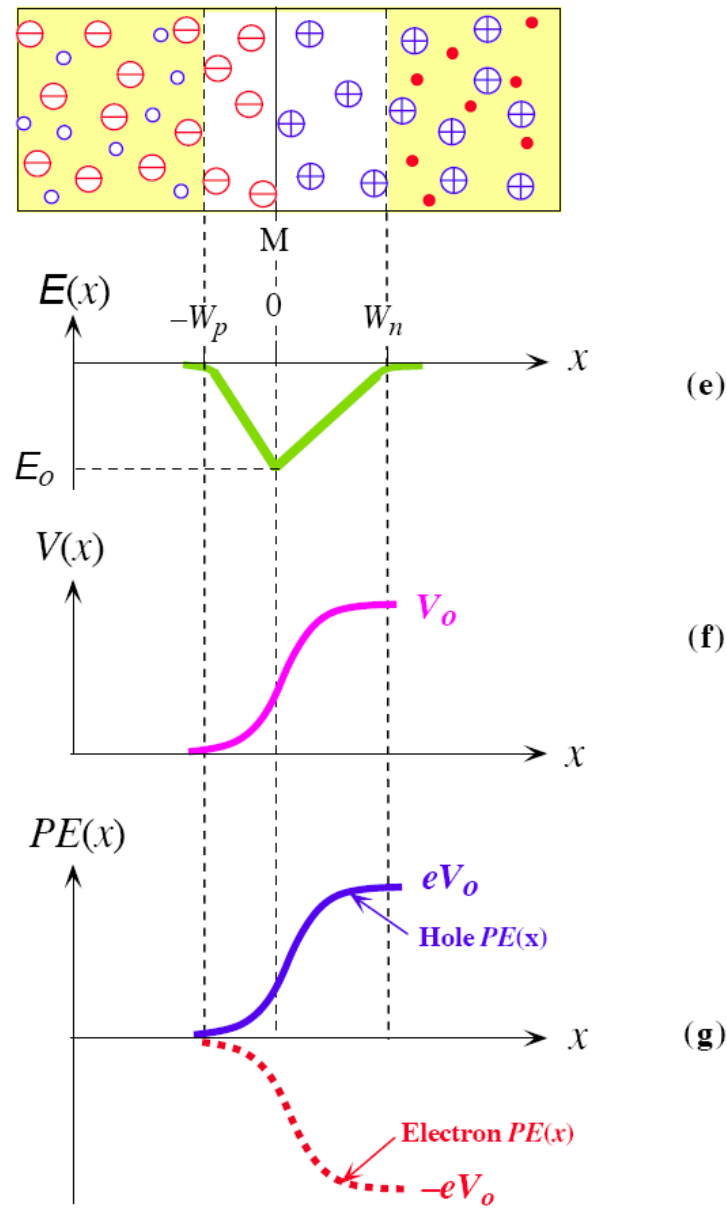


Fig 6.1

# Ideal *pn* Junction

Acceptor concentration

Donor concentration

Depletion Widths

$$N_a W_p = N_d W_n$$

Field (*E*) and net space charge density

Net space charge density

$$\frac{dE}{dx} = \frac{\rho_{\text{net}}(x)}{\epsilon}$$

Permittivity of the medium

Field in depletion region

$$E(x) = \frac{1}{\epsilon} \int_{-W_p}^x \rho_{\text{net}}(x) dx$$

Electric Field

# Ideal *pn* Junction

## Built-in field

$$\mathcal{E}_o = -\frac{eN_d W_n}{\varepsilon} \quad \text{where } \varepsilon = \varepsilon_o \varepsilon_r$$

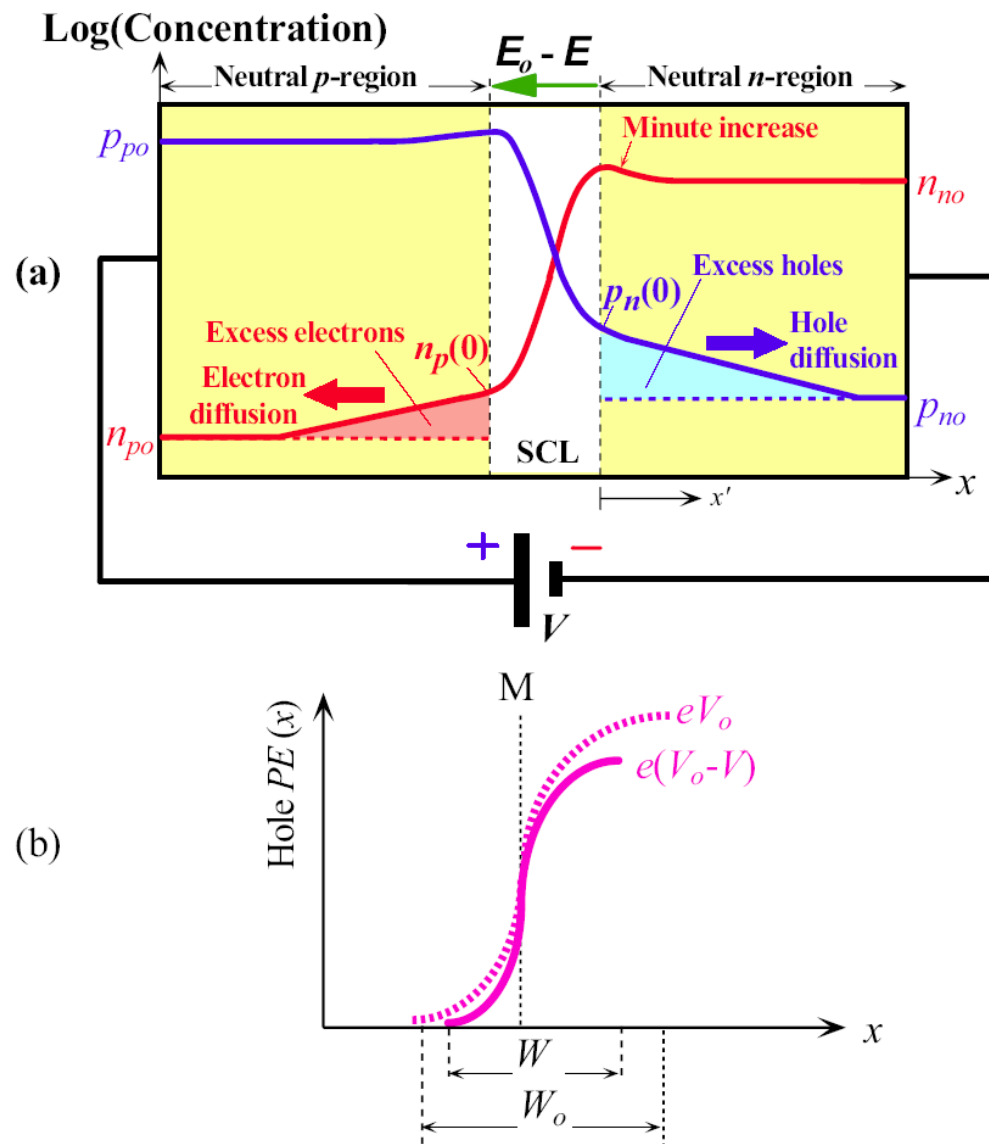
## Built-in voltage

$$V_o = \frac{kT}{e} \ln \left( \frac{N_a N_d}{n_i^2} \right) \quad \text{where } n_i \text{ is the intrinsic concentration}$$

## Depletion region width

$$W_o = \left[ \frac{2\varepsilon (N_a + N_d) V_o}{eN_a N_d} \right]^{1/2}$$

where  $W_o = W_n + W_p$  is the total width of the depletion region under a zero applied voltage



Forward biased  $pn$  junction and the injection of minority carriers.

(a) Carrier concentration profiles across the device under forward bias.

(b) The hole potential energy with and without an applied bias.  $W$  is the width of the SCL with forward bias.

Fig 6.2

# Forward Bias: Diffusion Current

## Law of the Junction: Minority Carrier Concentrations and Voltage

$$p_n(0) = p_{no} \exp\left(\frac{eV}{kT}\right)$$

$$n_p(0) = n_{po} \exp\left(\frac{eV}{kT}\right)$$

$p_n(0)$  is the hole concentration just outside the depletion region on the  $n$ -side

$n_p(0)$  is the electron concentration just outside the depletion region on the  $p$ -side



# Forward Bias: Diffusion Current

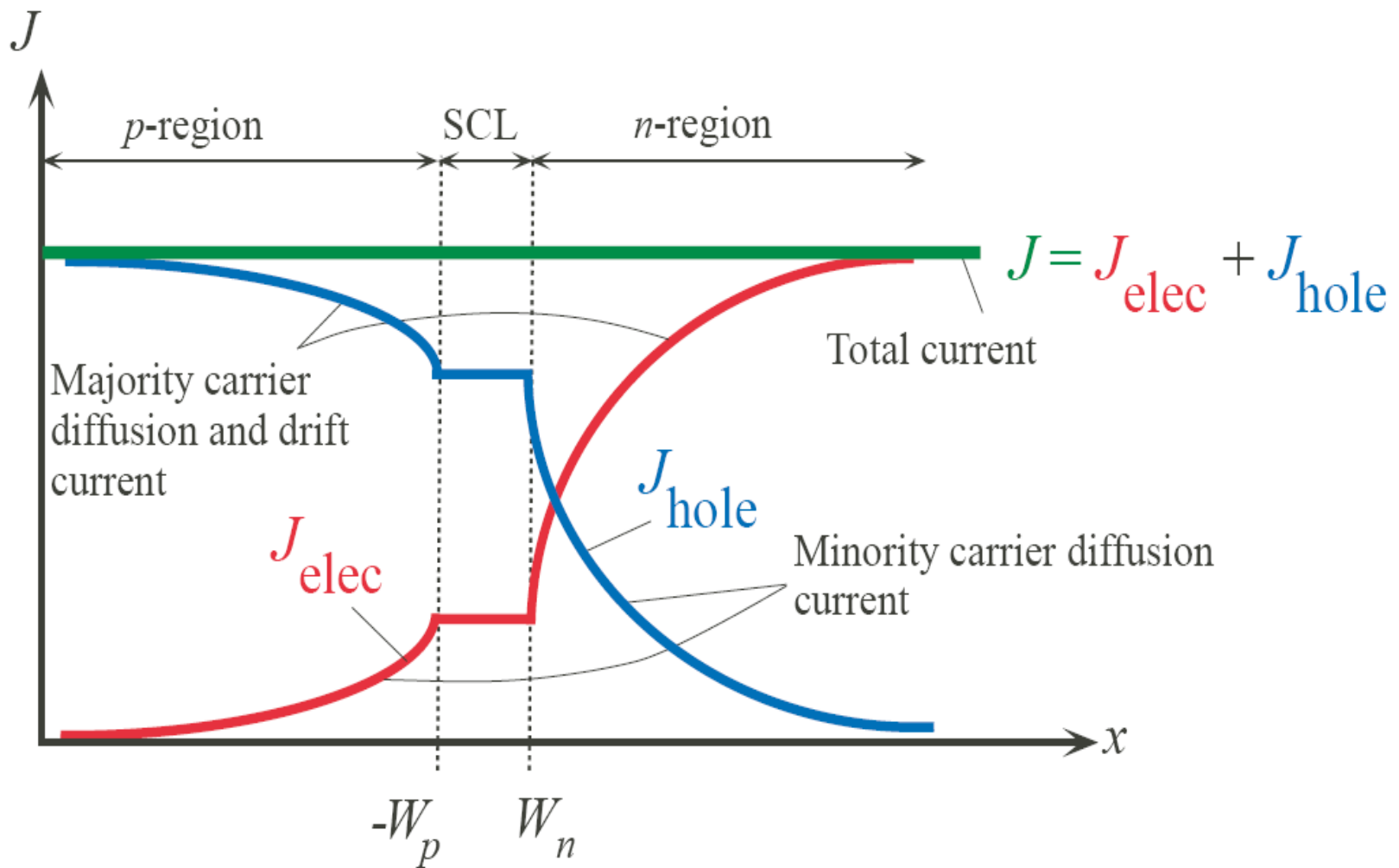
## Excess minority carrier concentration profile

$$\Delta p_n(x') = \Delta p_n(0) \exp\left(-\frac{x'}{L_h}\right)$$

where  $L_h$  is the hole diffusion length, defined by  $L_h = \sqrt{D_h \tau_h}$  in which  $\tau_h$  is the mean hole recombination lifetime (minority carrier lifetime in the  $n$ -region).

## Excess minority carrier concentration

$$\Delta p_n(x') = p_n(x') - p_{no}$$



The total current anywhere in the device is constant. Just outside the depletion region it is due to the diffusion of minority carriers.

Fig 6.3

# Forward Bias: Diffusion Current

Hole diffusion current in  $n$ -side in the neutral region

$$J_{D,\text{hole}} = \left( \frac{eD_h n_i^2}{L_h N_d} \right) \left[ \exp\left( \frac{eV}{kT} \right) - 1 \right]$$

There is a similar expression for the electron diffusion current density  $J_{D,\text{elec}}$  in the  $p$ -region.

# Forward Bias: Diffusion Current

Ideal diode (Shockley) equation

$$J = J_{so} \left[ \exp\left(\frac{eV}{kT}\right) - 1 \right]$$

Reverse saturation current

$$J_{so} = \left[ \left( \frac{eD_h}{L_h N_d} \right) + \left( \frac{eD_e}{L_e N_a} \right) \right] n_i^2$$

# Forward Bias: Diffusion Current

## Intrinsic concentration

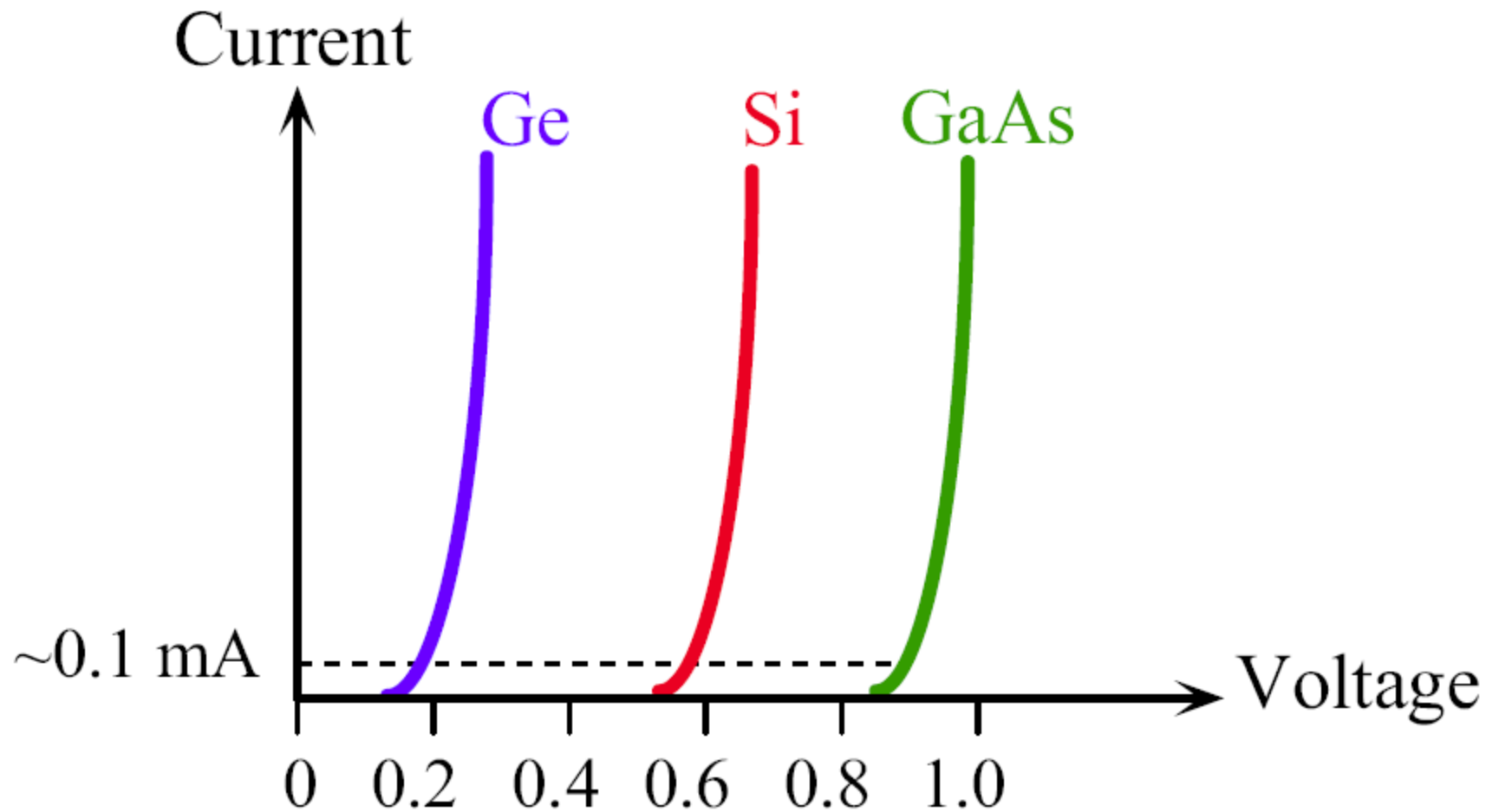
$$n_i^2 = (N_c N_v) \exp\left(-\frac{eV_g}{kT}\right)$$

where  $V_g = E_g / e$  is the bandgap energy expressed in volts

$V_g = 0.67$  V for Ge, 1.1 V for Si, and 1.42 V for GaAs

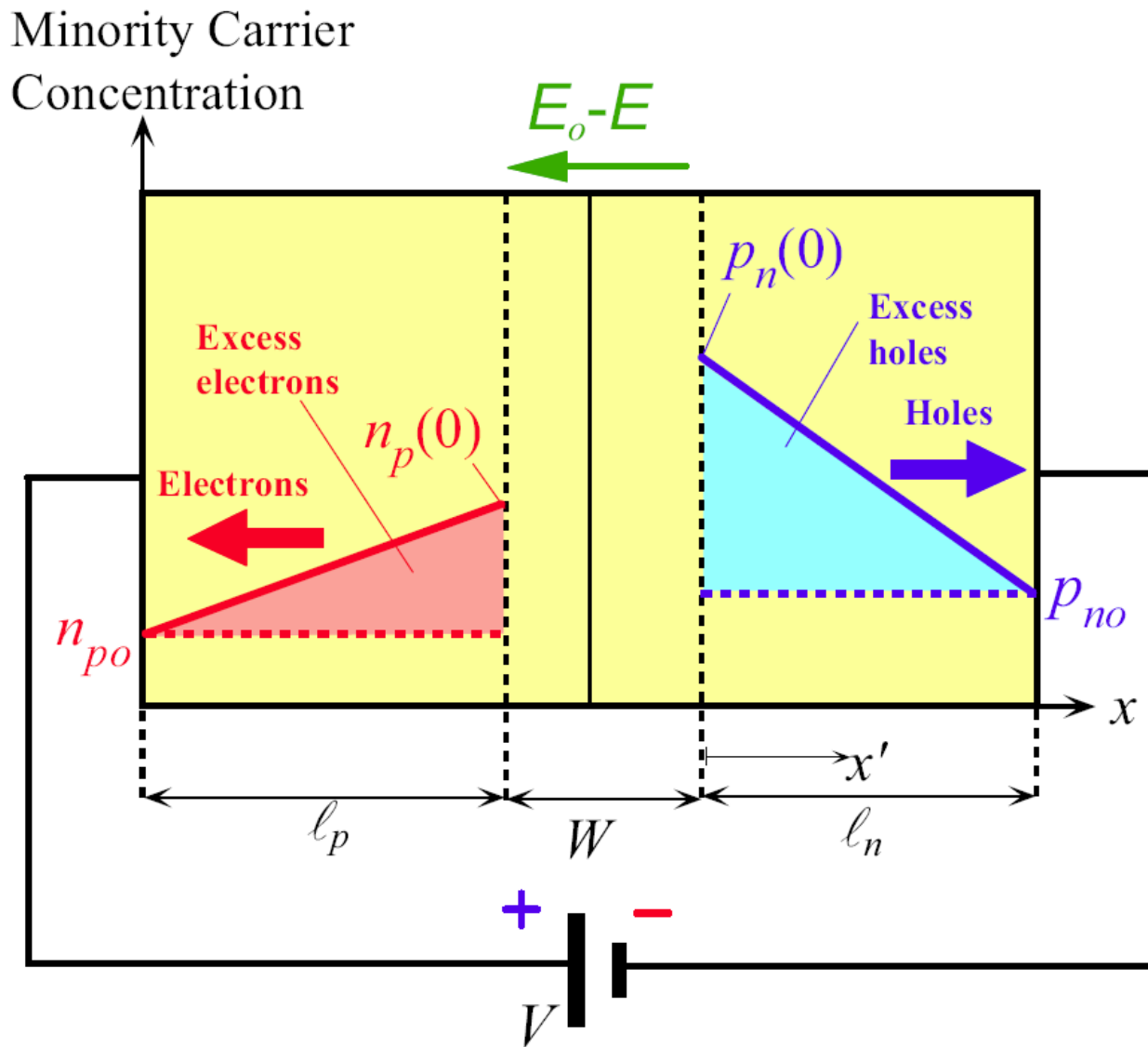
$$J = J_{so} \exp\left(\frac{eV}{kT}\right) = C \exp\left(\frac{e(V - V_g)}{kT}\right) \quad V > kT/e$$

We can plot  $I$  vs.  $V$  for Ge, Si and Ge



Schematic sketch of the I-V characteristics of Ge, Si, and GaAs pn junctions.

Fig 6.4



Minority carrier injection and diffusion in a short diode.

Fig 6.5

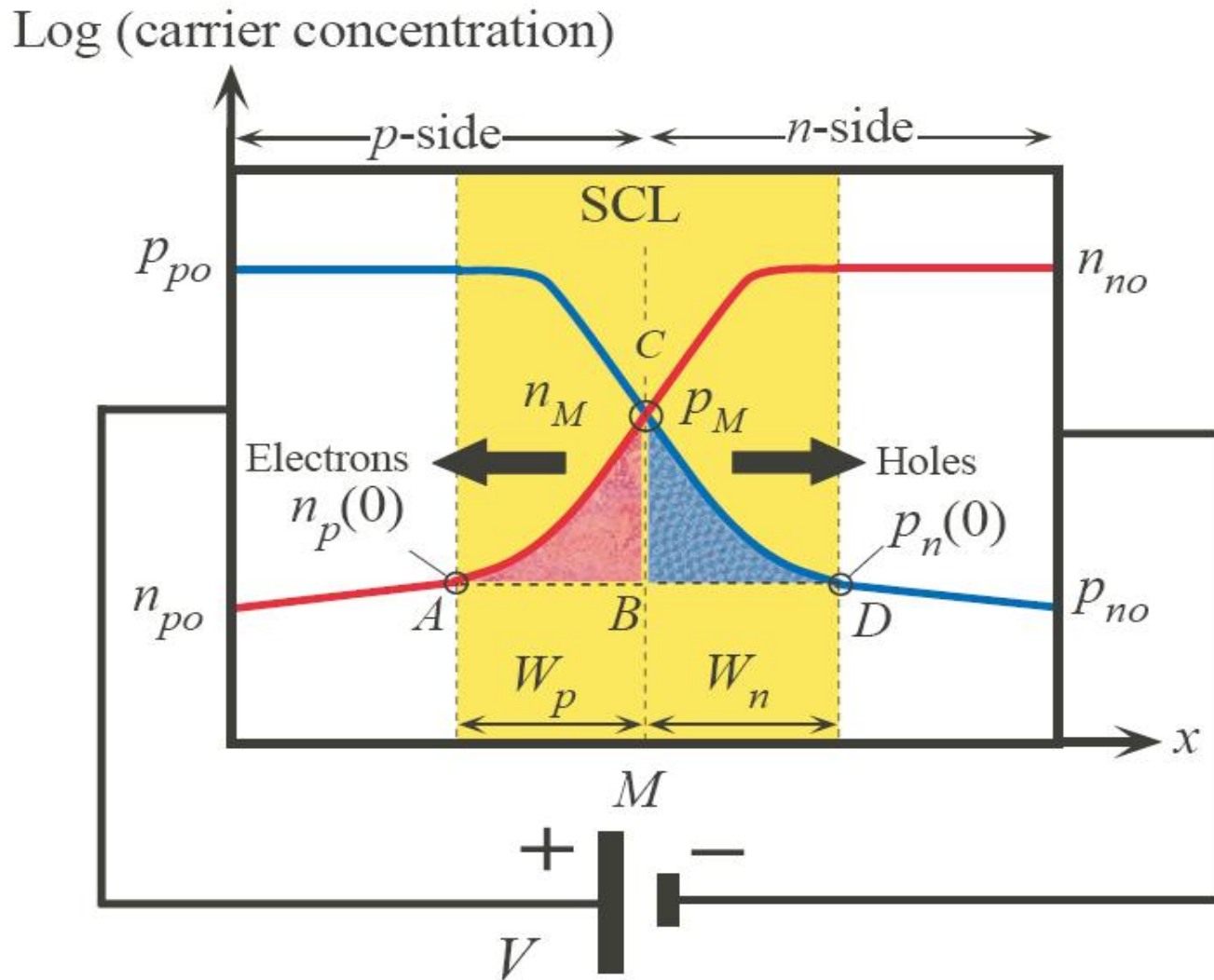
# Forward Bias: Diffusion Current

## Short Diode

$$J = \left( \frac{eD_h}{\ell_n N_d} + \frac{eD_e}{\ell_p N_a} \right) n_i^2 \left[ \exp\left(\frac{eV}{kT}\right) - 1 \right]$$

where  $\ell_n$  and  $\ell_p$  represent the lengths of the neutral  $n$ - and  $p$ -regions outside the depletion region.





Forward biased pn junction and the injection of carriers and their recombination in the SCL

Fig 6.6

# Forward Bias: Recombination and Total Current

## Recombination Current

$$J_{\text{recom}} = J_{ro} [\exp(eV / 2kT) - 1] \quad \text{where } J_{ro} = \frac{en_i}{2} \left( \frac{W_p}{\tau_e} + \frac{W_n}{\tau_h} \right)$$

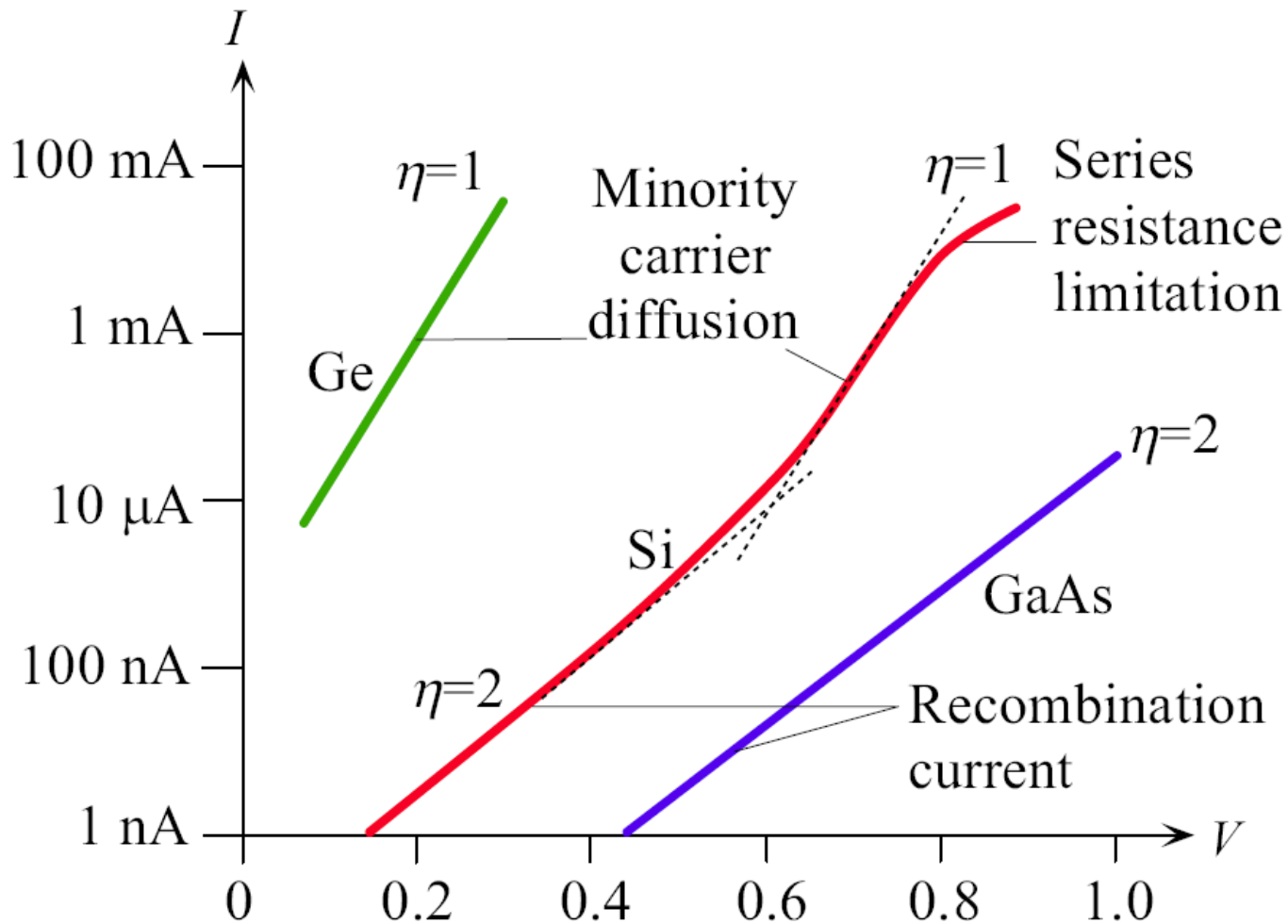
**Total diode current = diffusion + recombination**

$$J = J_{so} \exp\left(\frac{eV}{kT}\right) + J_{ro} \exp\left(\frac{eV}{2kT}\right) \quad V > \frac{kT}{e}$$

**The diode equation**

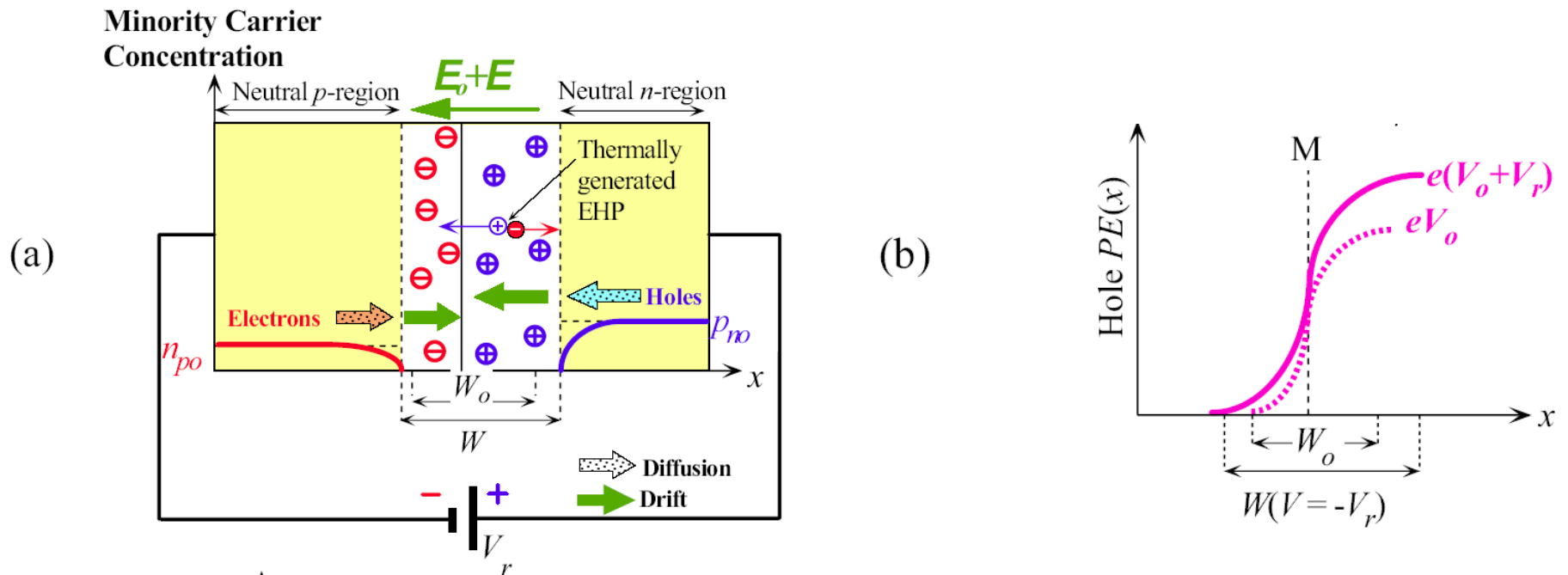
$$J = J_o \exp\left(\frac{eV}{\eta kT}\right) \quad V > \frac{kT}{e}$$

Where  $J_o$  is a new constant and  $\eta$  is an ideality factor



Schematic sketch of typical  $I$ - $V$  characteristics of Ge, Si and GaAs pn junctions as  $\log(I)$  vs.  $V$ . The slope indicates  $e/(\eta kT)$

Fig 6.7



Reverse biased pn junction. (a) Minority carrier profiles and the origin of the reverse current. (b) Hole PE across the junction under reverse bias

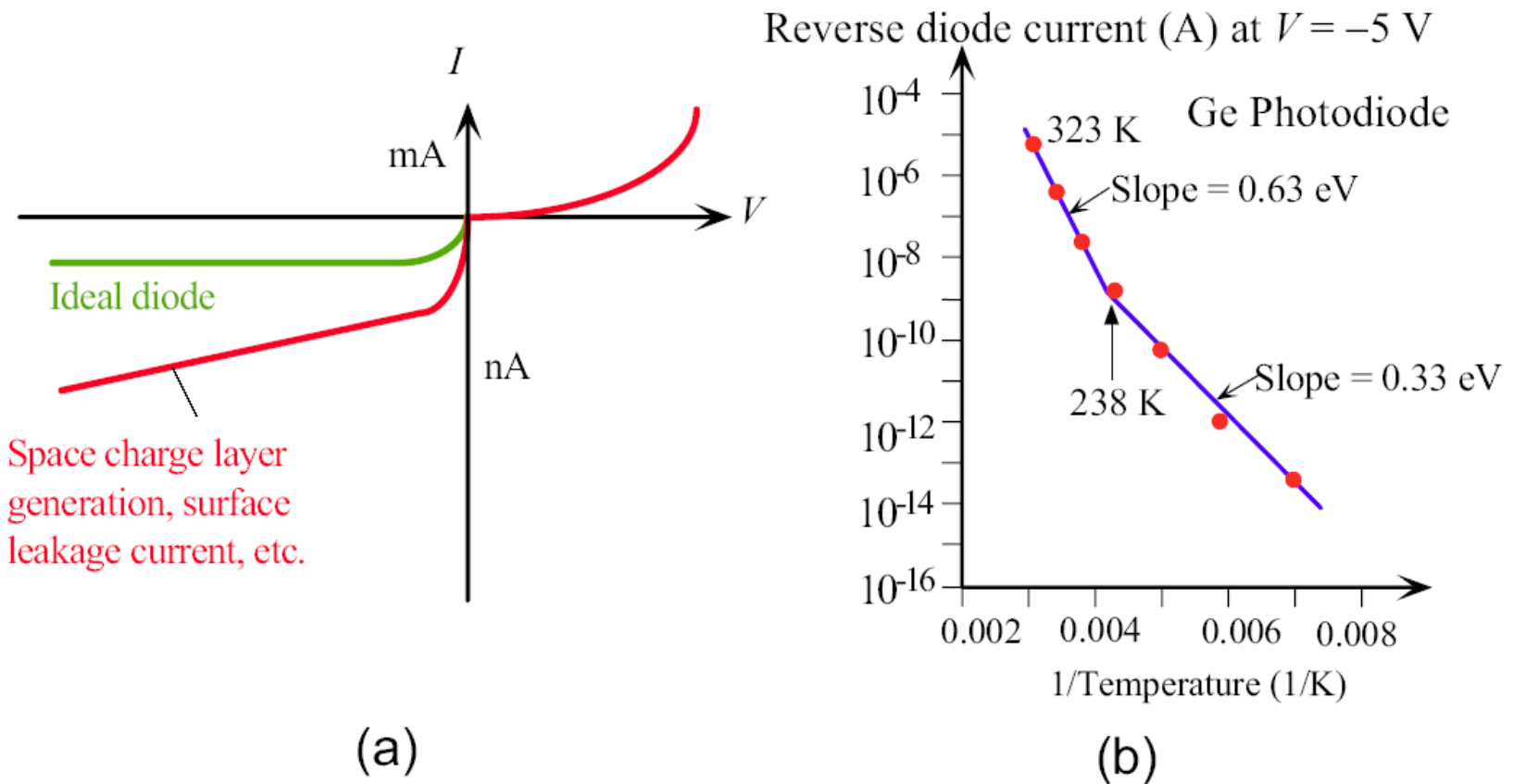
Fig 6.8

# Reverse Bias

## Total Reverse Current

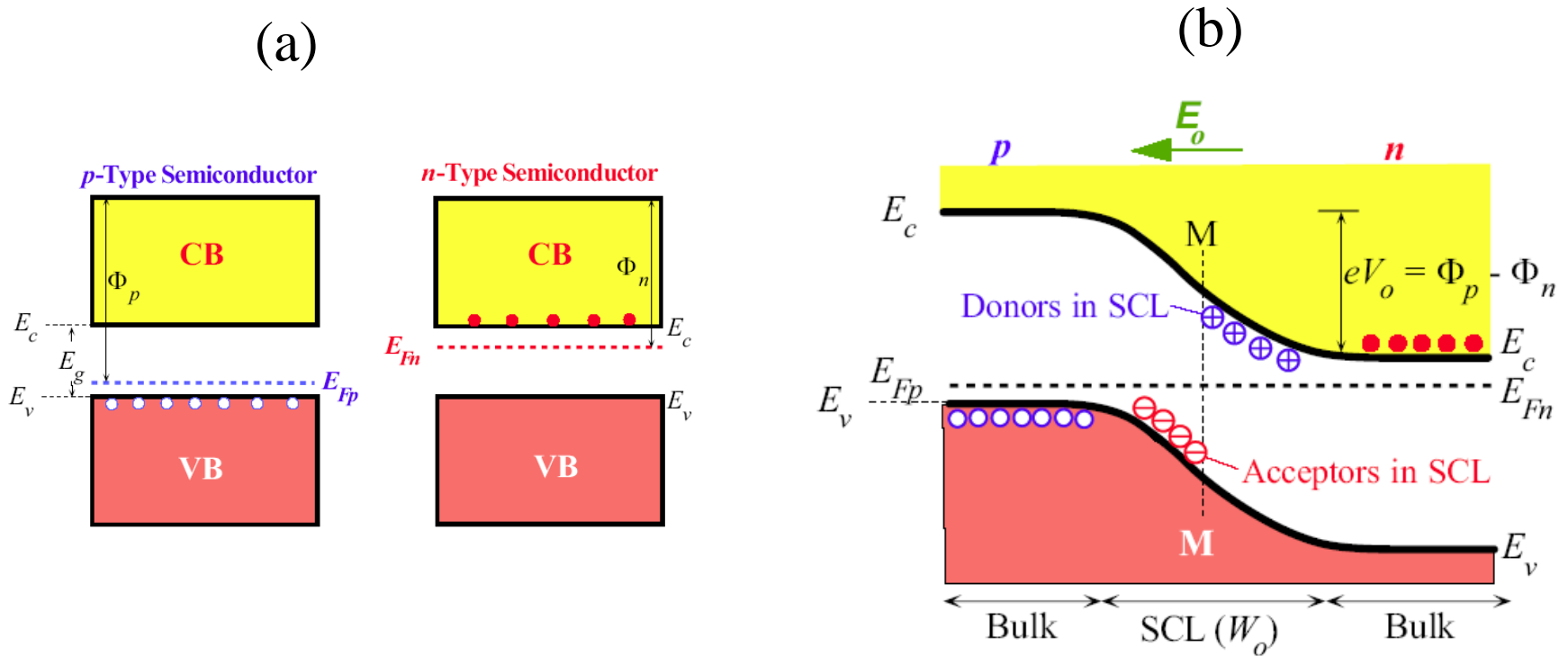
Thermal generation in depletion region  
↓

$$J_{\text{rev}} = \underbrace{\left( \frac{eD_h}{L_h N_d} + \frac{eD_e}{L_e N_a} \right) n_i^2}_{\substack{\text{Diffusion current in neutral regions} \\ \text{the Shockley reverse current}}} + \underbrace{\frac{eWn_i}{\tau_g}}_{\substack{\text{Mean thermal generation time}}}$$



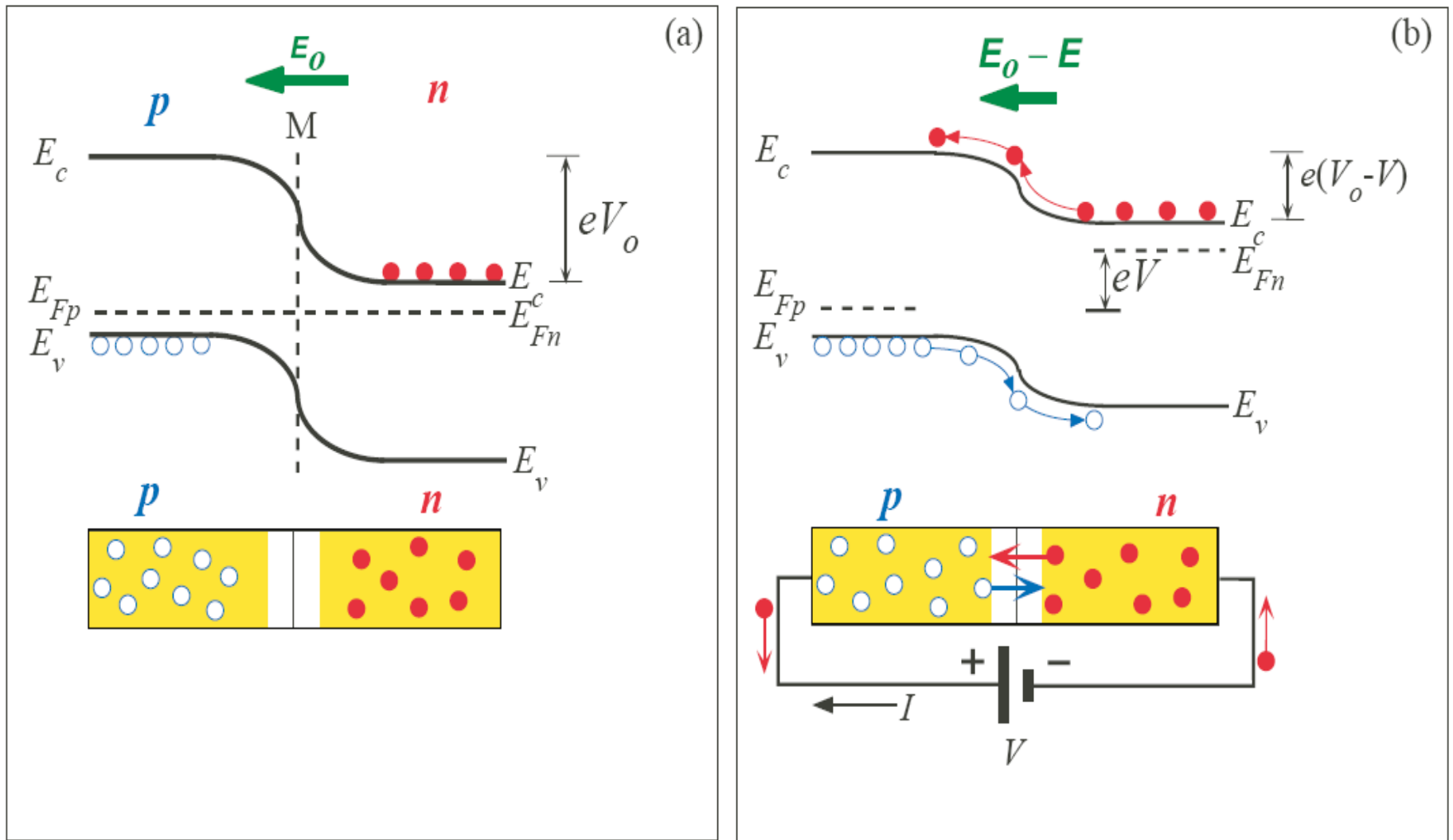
(a) Reverse I-V characteristics of a pn junction (the positive and negative current axes have different scales). (b) Reverse diode current in a Ge pn junction as a function of temperature in a  $\ln(I_{\text{rev}})$  vs  $1/T$  plot. Above  $238$  K,  $I_{\text{rev}}$  is controlled by  $n_i^2$  and below  $238$  K it is controlled by  $n_i$ . The vertical axis is a logarithmic scale with actual current values. (From D. Scansen and S.O. Kasap, *Cnd. J. Physics*. **70**, 1070-1075, 1992.)

Fig 6.9



- (a) Two isolated  $p$  and  $n$ -type semiconductors (same material).
- (b) A pn junction band diagram when the two semiconductors are in contact. The Fermi level must be uniform in equilibrium. The metallurgical junction is at M. The region around M contains the space charge layer (SCL). On the  $n$ -side of M, SCL has the exposed positively charged donors whereas on the  $p$ -side it has the exposed negatively charged acceptors.

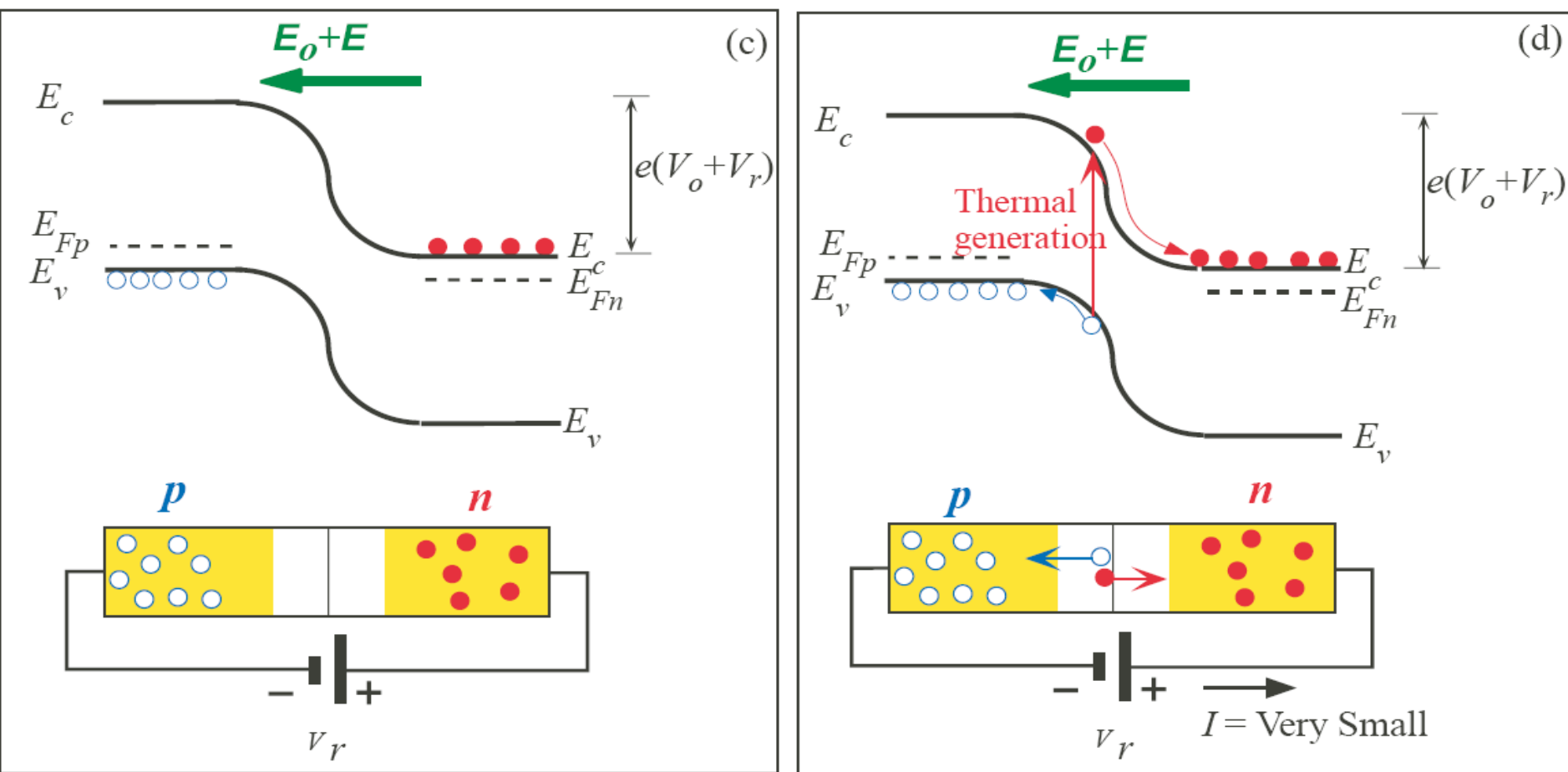
Fig 6.10



Energy band diagrams for a pn junction under  
 (a) open circuit and (b) forward bias

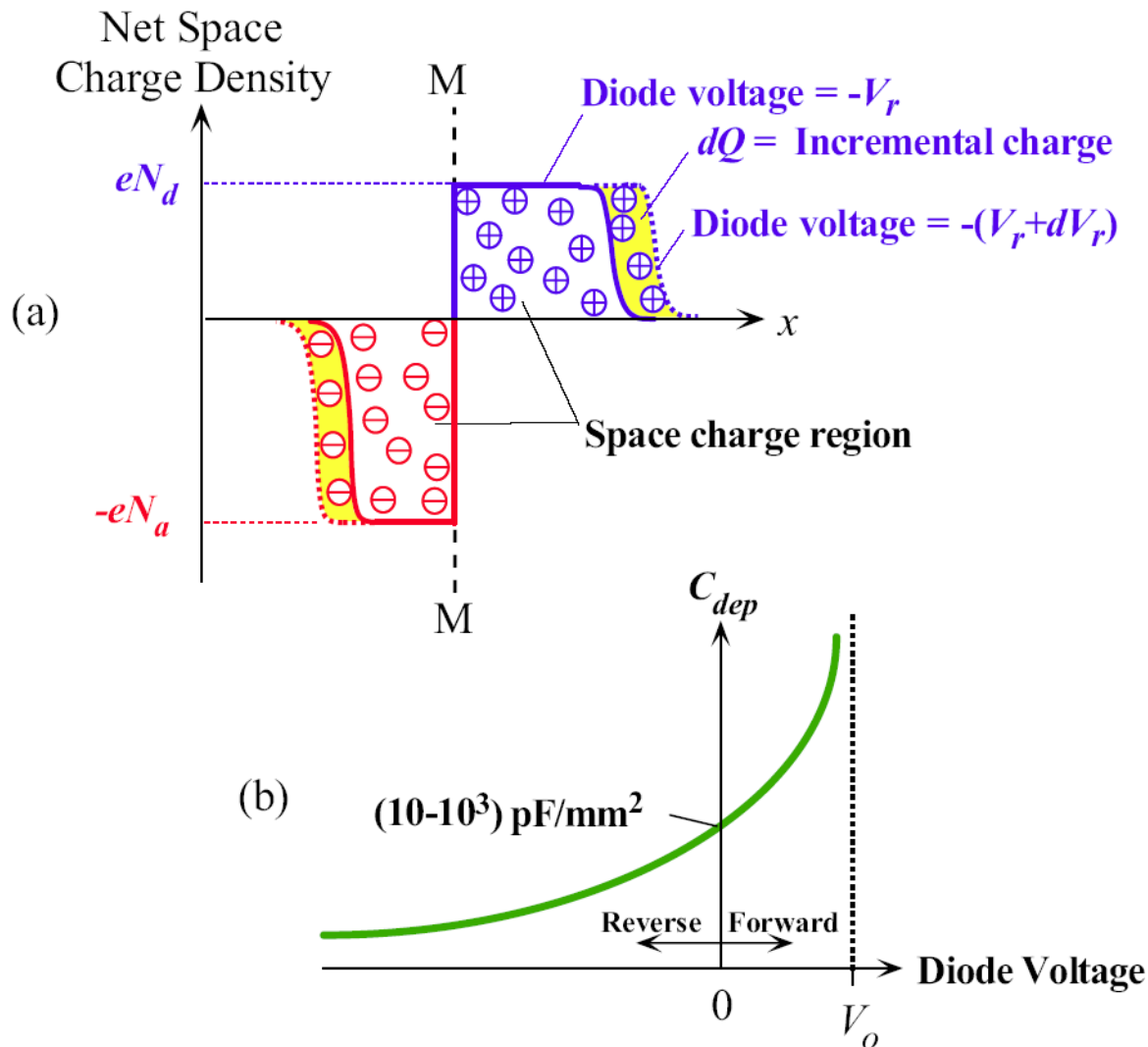
Fig 6.11





Energy band diagrams for a pn junction under (c) reverse bias conditions; and (d) thermal generation of electron hole pairs in the depletion region results in a small reverse current.

Fig 6.11



The depletion region behaves like a capacitor.

(a) The charge in the depletion region depends on the applied voltage just as in a capacitor

(b) The incremental capacitances of the depletion region increases with forward bias and decreases with reverse bias. Its value is typically in the range of picofarads per  $\text{mm}^2$

Fig 6.12

# Depletion layer capacitance of the pn junction

## Depletion region width

$$W = \left[ \frac{2\epsilon (N_a + N_d) (V_o - V)}{e N_a N_d} \right]^{1/2}$$

where, for forward bias,  $V$  is positive, which reduces  $V_o$ , and, for reverse bias,  $V$  is negative, so  $V_o$  is increased.

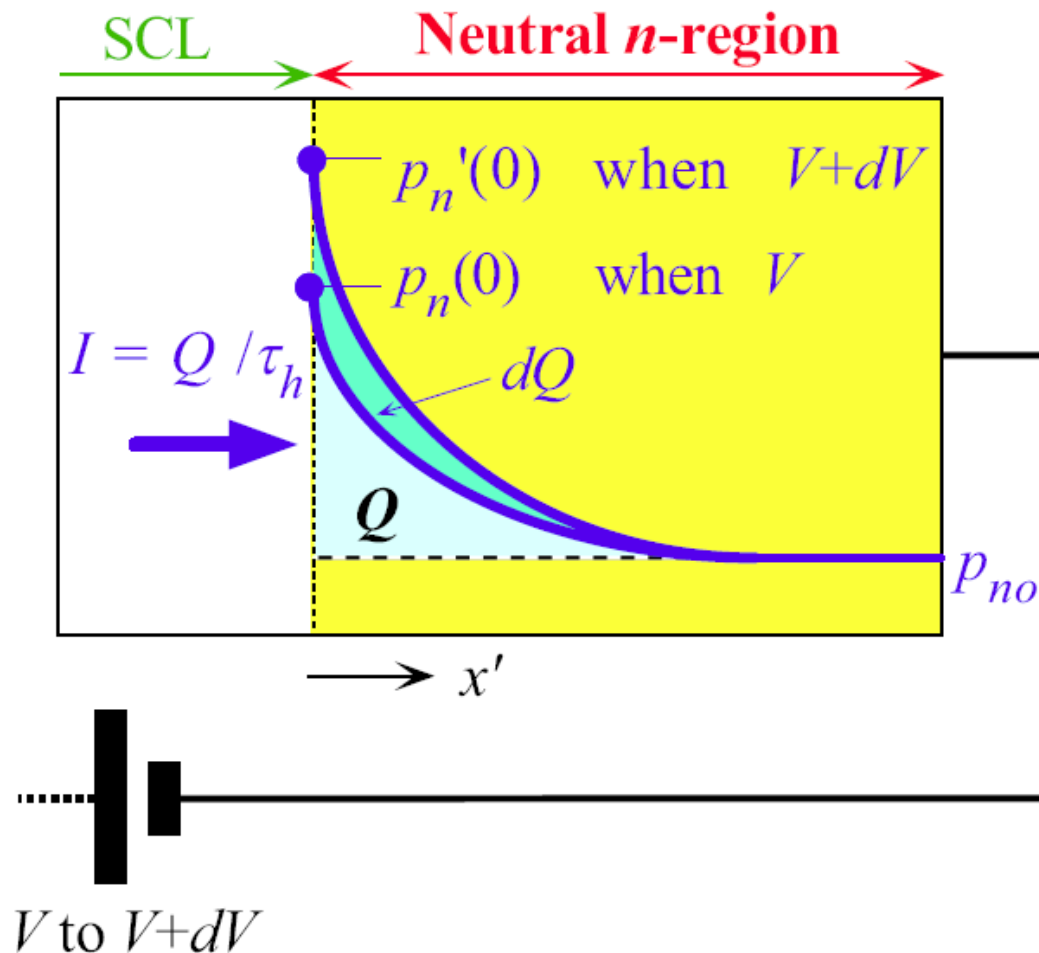
## Definition of depletion layer capacitance $C_{\text{dep}}$

$$C_{\text{dep}} = \left| \frac{dQ}{dV} \right|$$

where the amount of charge on any one side of the depletion layer is  $|Q| = eN_d W_n A = eN_a W_p A$  and  $W = W_n + W_p$

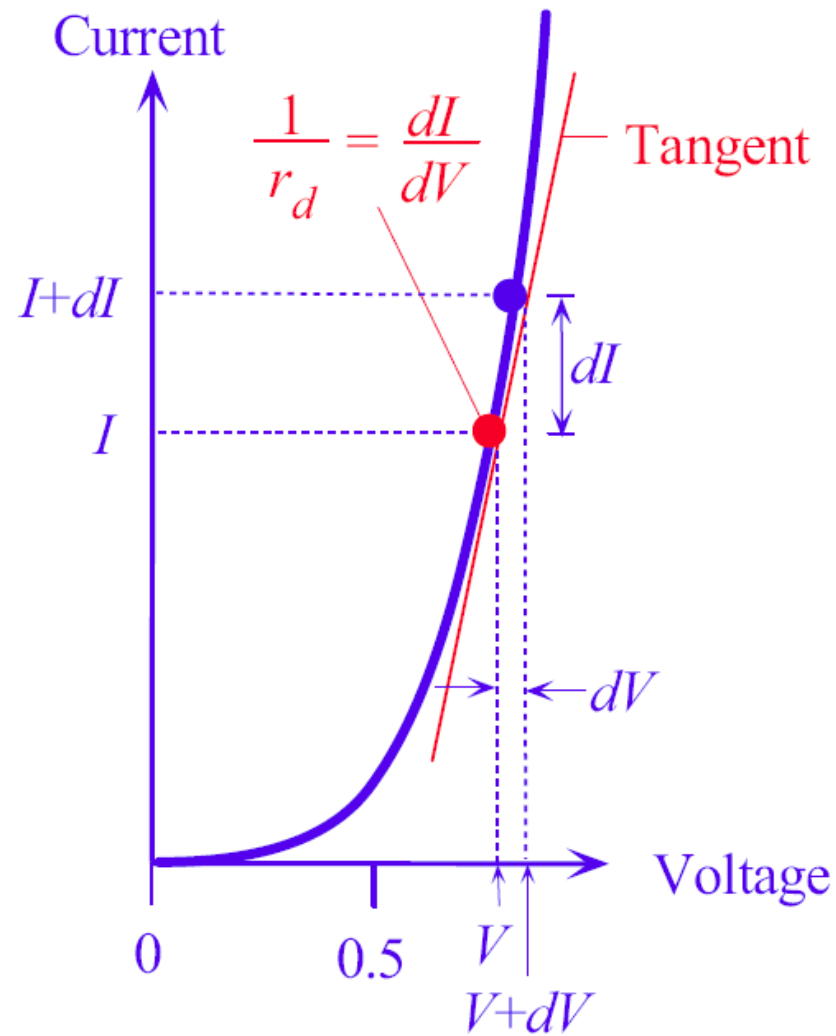
# Depletion Capacitance

$$C_{\text{dep}} = \frac{\epsilon A}{W} = \frac{A}{\sqrt{V_o - V}} \left[ \frac{e \epsilon N_a N_d}{2(N_a + N_d)} \right]^{1/2}$$



Consider the injection of holes into the  $n$ -side during forward bias. Storage or diffusion capacitance arises because when the diode voltage increases from  $V$  to  $V+dV$  then more minority carriers are injected and more minority carrier charge is stored in the  $n$ -region.

Fig 6.13



The dynamic resistance of the diode is defined as  $dV/dI$  which is the inverse of the tangent at  $I$ .

Fig 6.14

# Diffusion capacitance and dynamic resistance

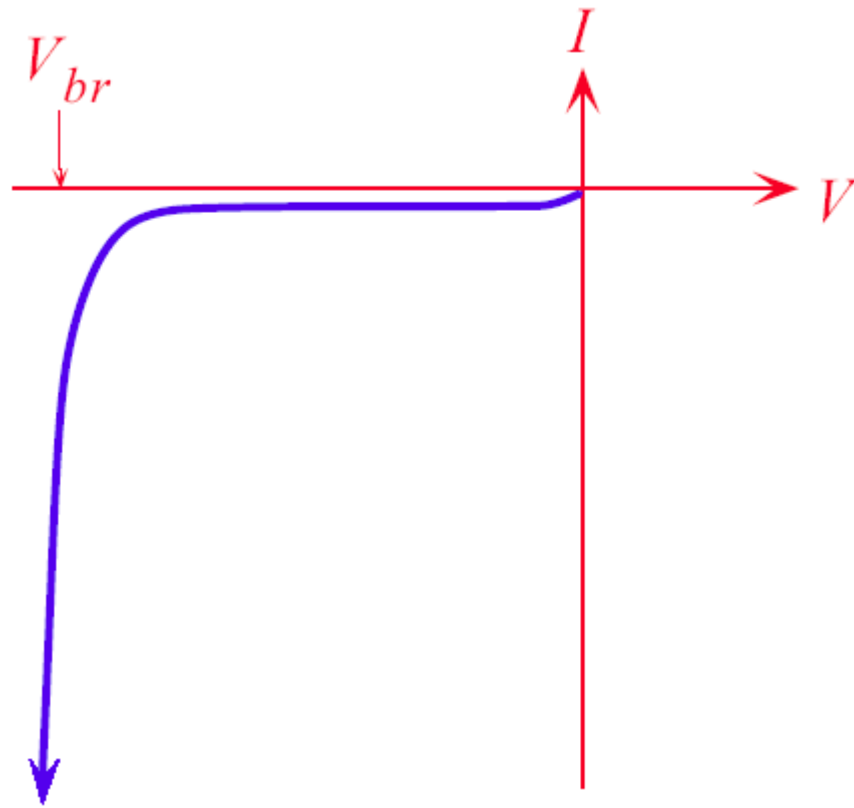
## Diffusion capacitance

$$C_{\text{diff}} = \frac{dQ}{dV} = \frac{\tau_h e I}{kT} = \frac{\tau_h I (\text{mA})}{25}$$

where we used  $e/kT \approx 40 = 1/0.025$  at room temperature

## Dynamic incremental resistance

$$r_d = \frac{dV}{dI} = \frac{kT}{eI} = \frac{25}{I(\text{mA})}$$



Reverse  $I$ - $V$  characteristics of a  $pn$  junction.

Fig 6.15



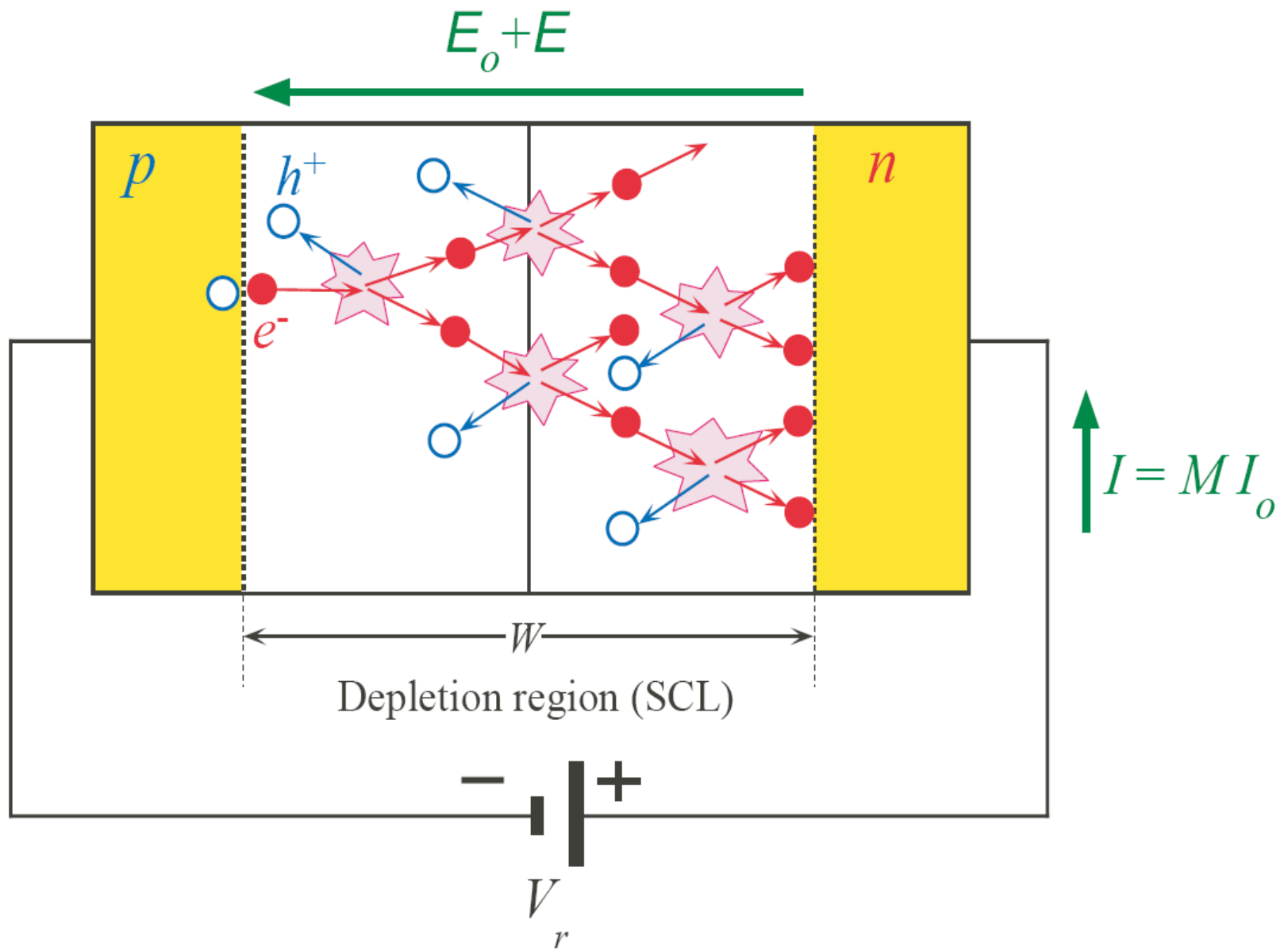
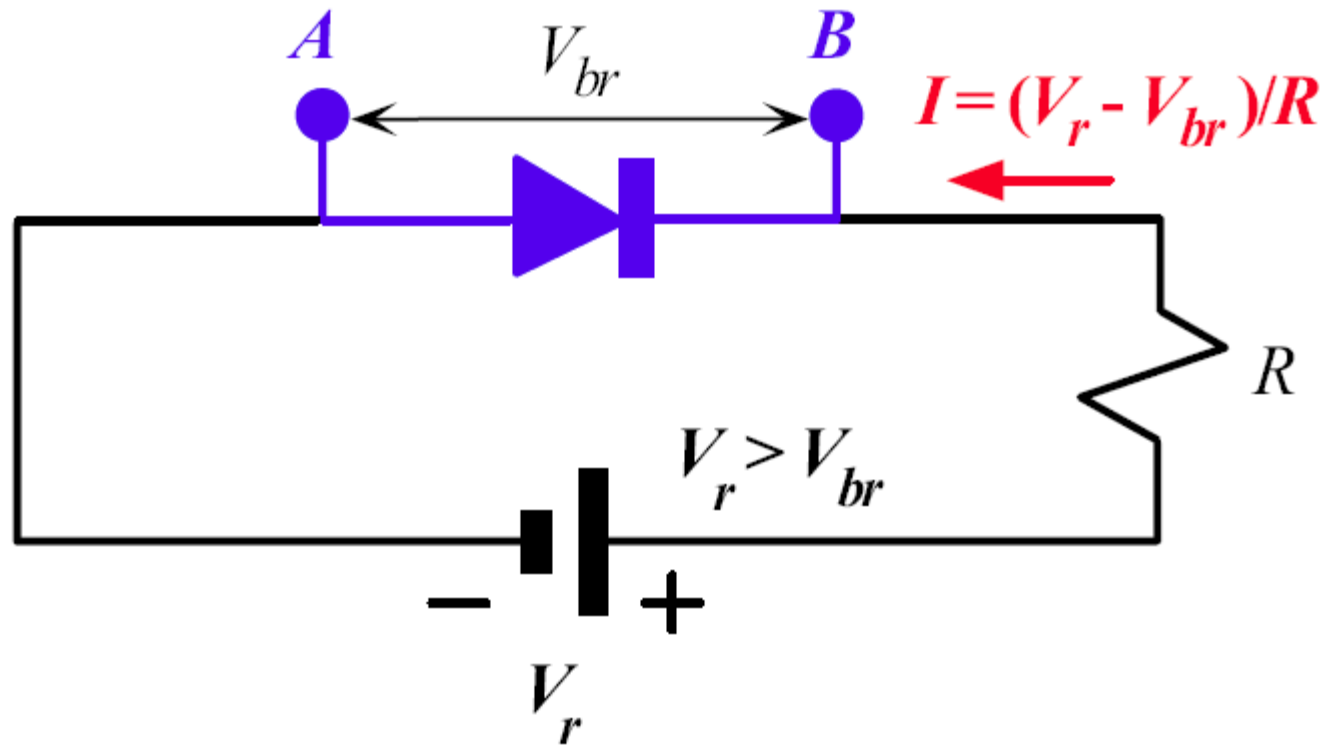
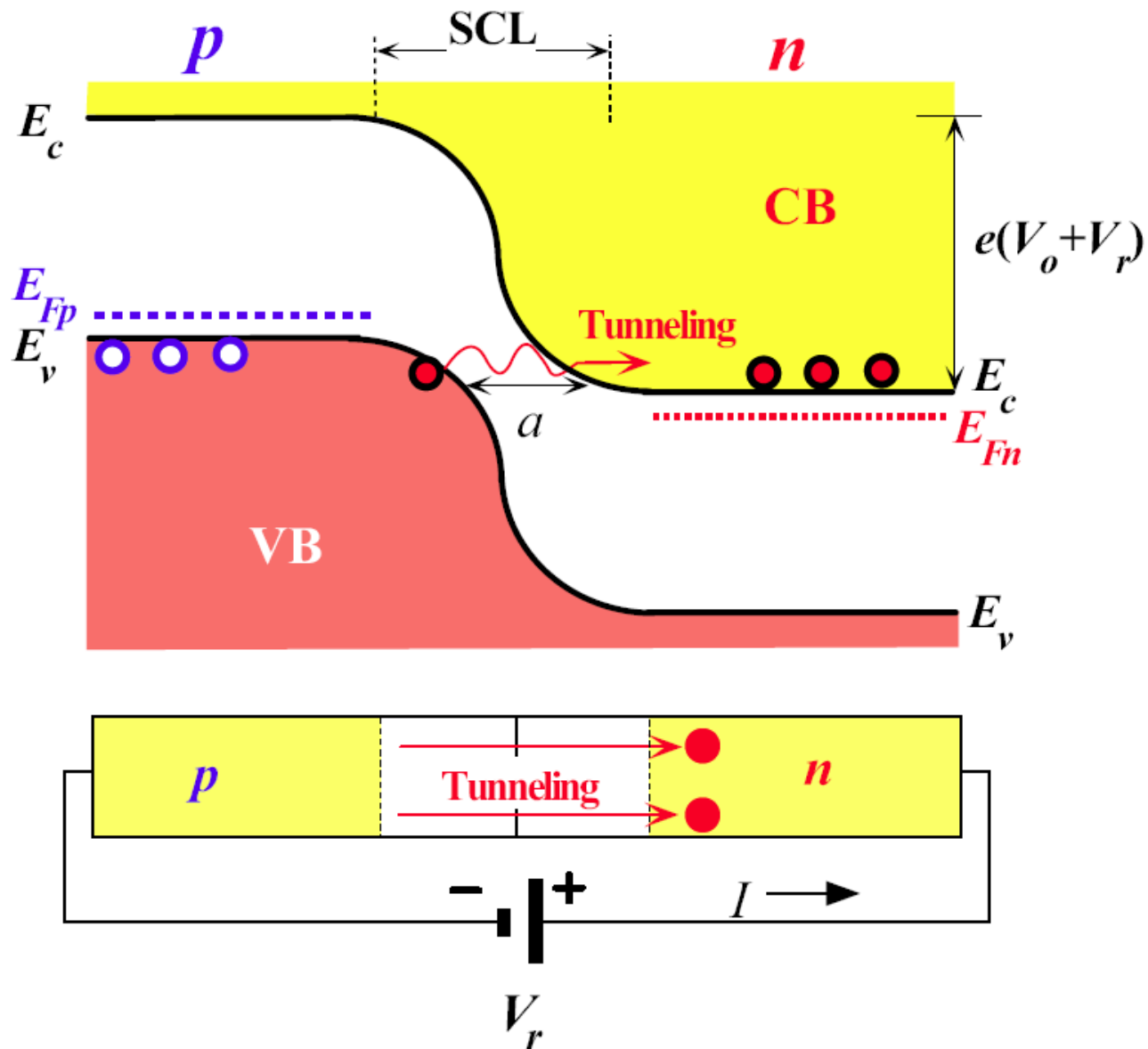


Fig 6.16



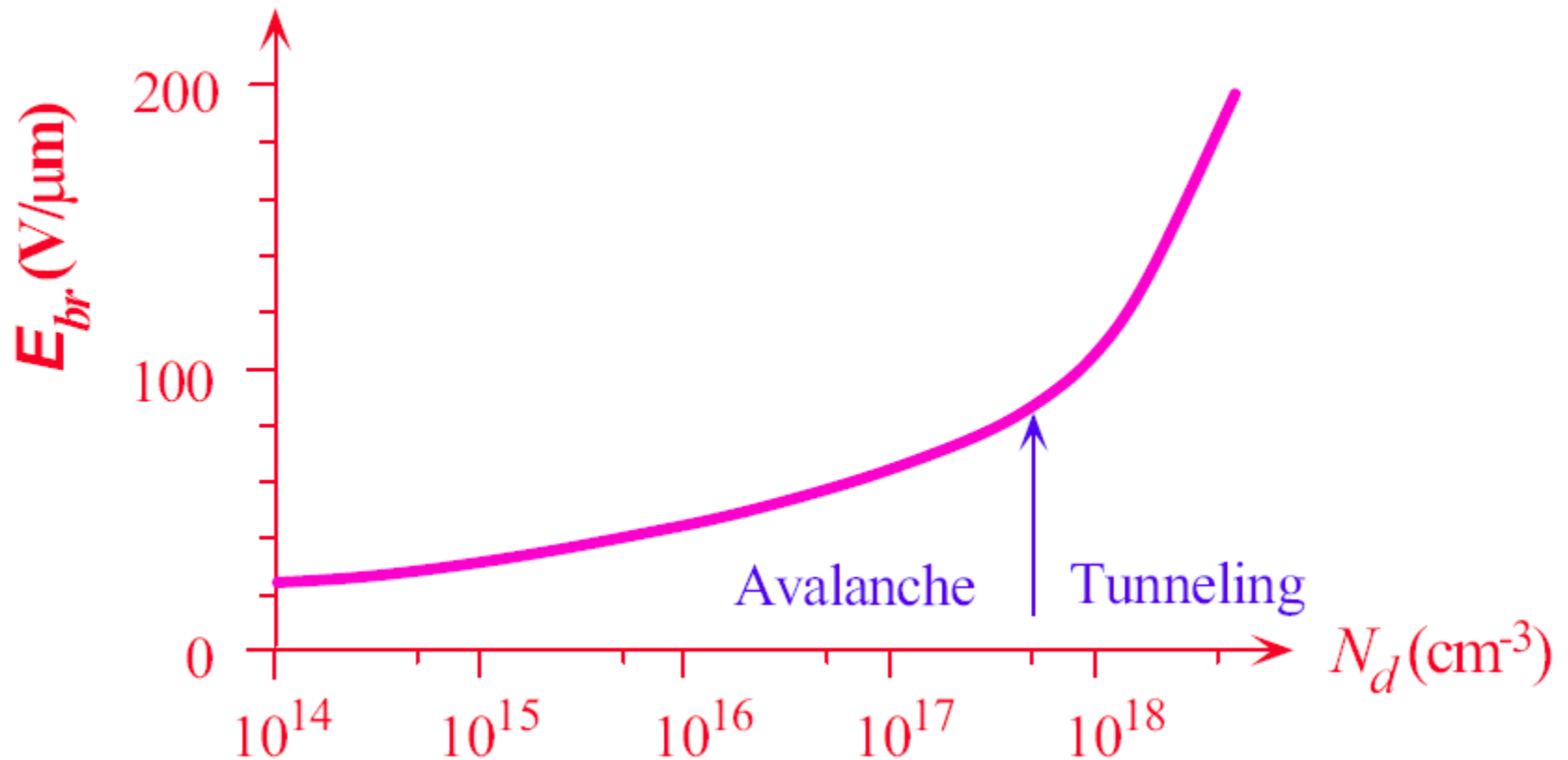
If the reverse breakdown current when  $V_r > V_{br}$  is limited by an external resistance,  $R$ , to prevent destructive power dissipation then the diode can be used to clamp the voltage between  $A$  and  $B$  to remain approximately  $V_{br}$ .

Fig 6.17



Zener breakdown involves electrons tunneling from the VB of p side to the CB of  $n$ -side when the reverse bias reduces  $E_c$  to line up with  $E_v$ .

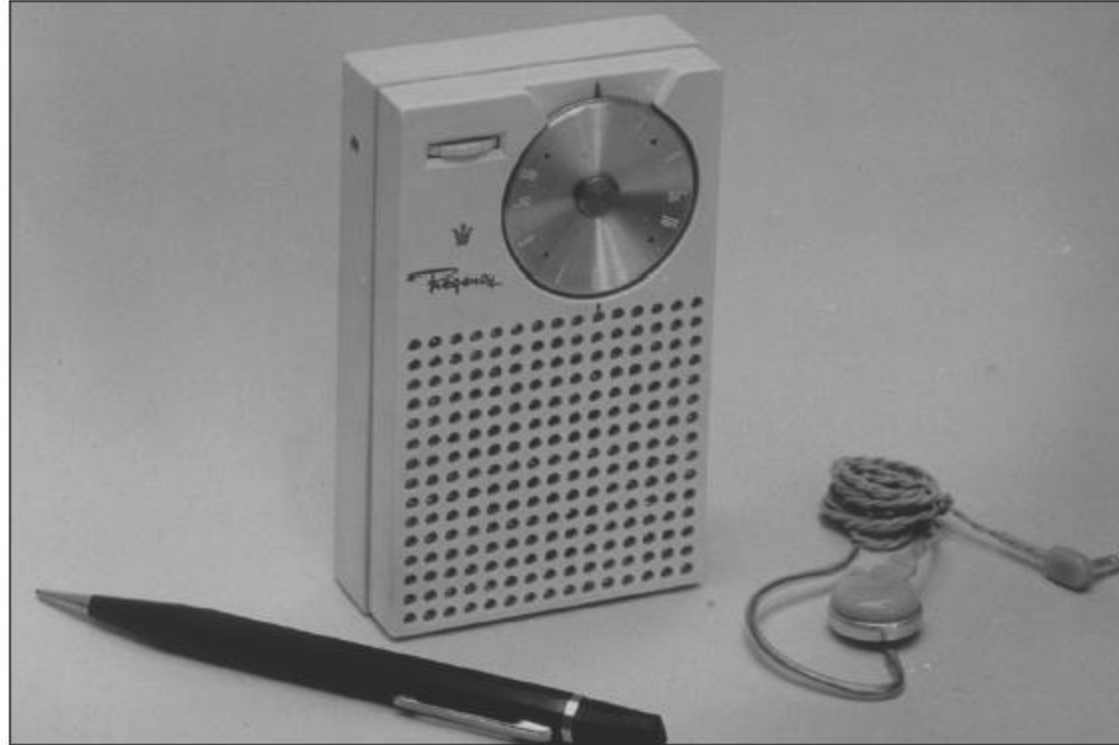
Fig 6.18



The breakdown field  $E_{br}$  in the depletion layer for the onset of reverse breakdown vs. doping concentration  $N_d$  in the lightly doped region in a one-sided ( $p^+n$  or  $pn^+$ ) abrupt pn junction. avalanche and tunneling mechanisms are separated by the arrow [data extracted from M.Sze and G. Gibbons, Solid. State. Electronics, 9, 831 (1966)]

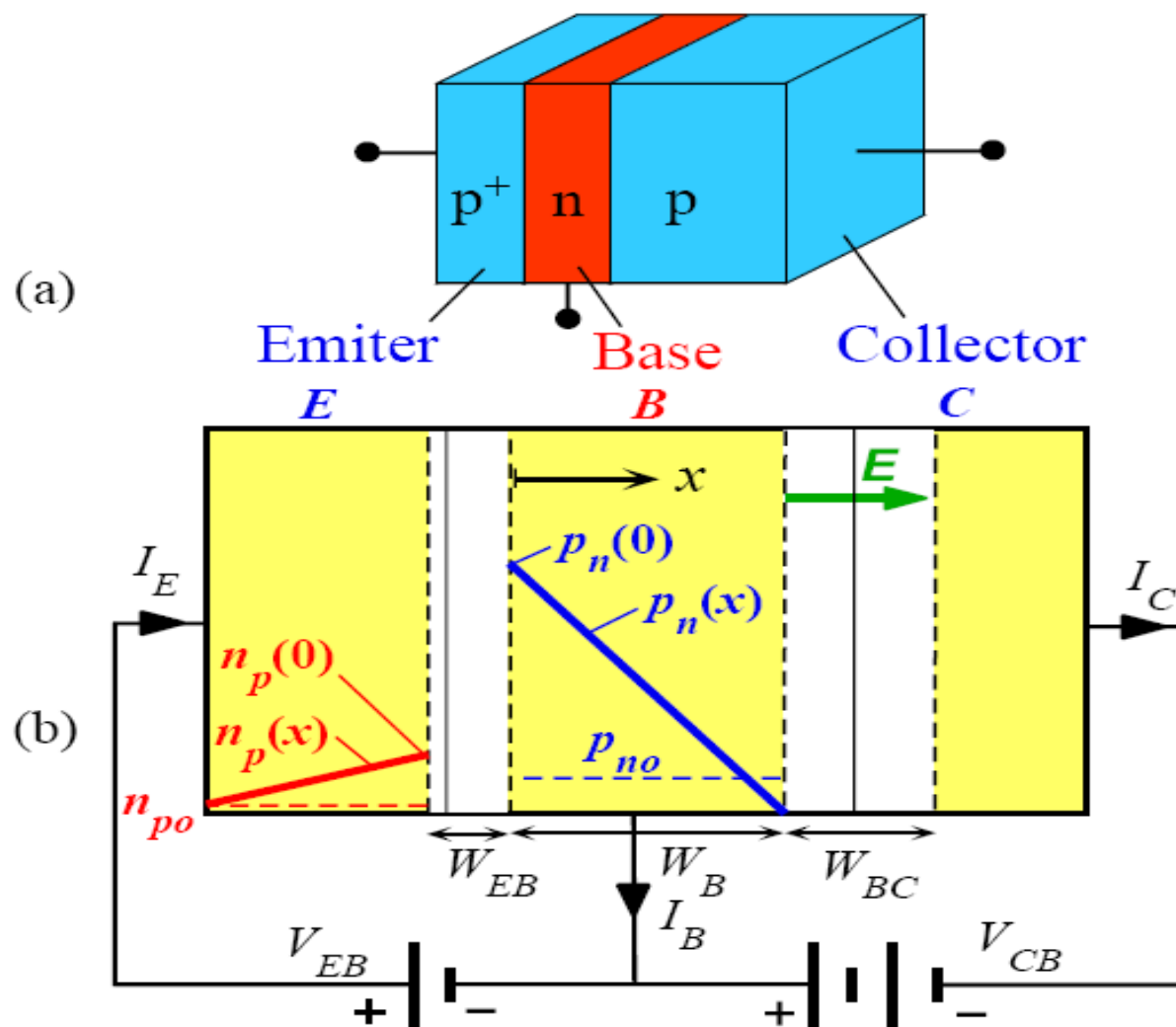
Fig 6.19

# The Bipolar Junction Transistor: BJT



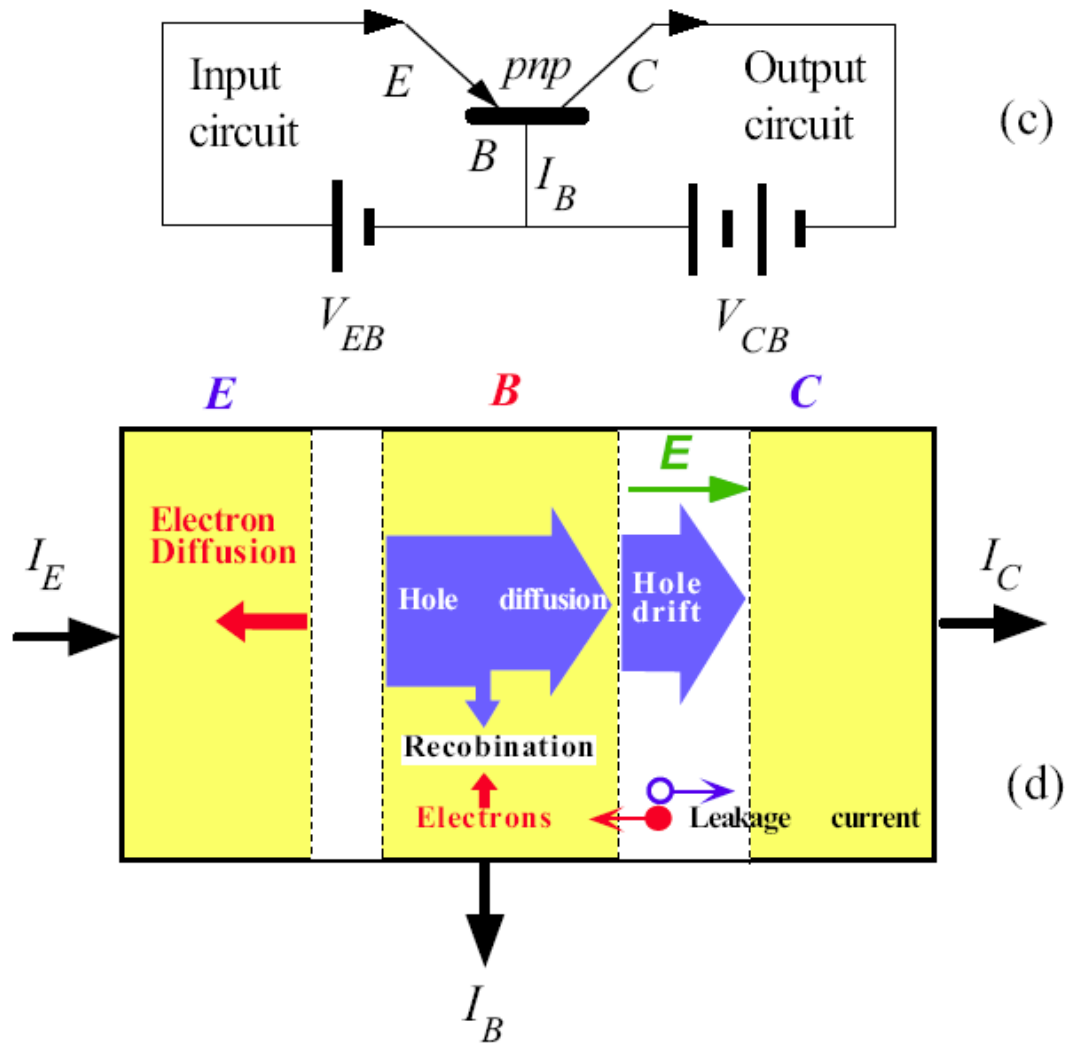
Left: The first commercial Si transistor from Texas Instruments (1954). Right: The first transistor pocket radio (1954). It had four Ge *nnp* transistors.

| SOURCE: Courtesy of Texas Instruments.



- (a) A schematic illustration of the *pnp* bipolar transistor with three differently doped regions.
- (b) The *pnp* bipolar operated under normal and active conditions.

Fig 6.20



(c) The CB configuration with input and output circuits identified.

(d) The illustration of various current components under normal and active conditions.

Fig 6.20

# Emitter Junction: The Law of the Junction

Hole concentration just outside the depletion region in the base at the emitter end

$$p_n(0) = p_{no} \exp\left(\frac{eV_{EB}}{kT}\right)$$

where  $V_{EB}$  is the forward bias applied across the emitter-base (EB) junction

Hole concentration just outside the depletion region in the base at the collector end

$$p_n(W_B) \approx 0$$



# The Emitter Current

Holes diffuse through the base, from the emitter end to the collector end. This diffusion is driven by the hole concentration gradient  $dp_n/dx$ .

Assume that the hole concentration profile is linear; it decreases from  $p_n(0)$  to 0 over the neutral base width  $W_B$ . (Initially, neglect the recombination of holes with electrons in the base.)

$$I_E = -eAD_h \left( \frac{dp_n}{dx} \right)_{x=0} = \frac{eAD_h p_n(0)}{W_B}$$

# BJT Common base (CB) dc characteristics

## Emitter Current

$$I_E = \frac{eAD_h p_{no}}{W_B} \exp\left(\frac{eV_{EB}}{kT}\right)$$

where  $V_{EB}$  is the forward bias applied across the emitter-base (EB) junction and  $W_B$  is the neutral base width.

## Definition of CB current gain

$$\alpha = \frac{I_C}{I_E}$$

Typically  $\alpha$  is less than unity, in the range 0.990 - 0.999

# BJT Common base dc characteristics

Total emitter current

$$I_E = I_{E(\text{hole})} + I_{E(\text{electron})}$$

Emitter injection efficiency

$$\gamma = \frac{I_{E(\text{hole})}}{I_{E(\text{hole})} + I_{E(\text{electron})}} = \frac{1}{1 + \frac{I_{E(\text{electron})}}{I_{E(\text{hole})}}}$$

# BJT Common base dc characteristics

## Definition of base transport factor $\alpha_T$

$$\alpha_T = \frac{I_C}{I_{E(\text{hole})}} = \frac{I_C}{\gamma I_E}$$

If the emitter were a perfect injector,  $I_E = I_{E(\text{hole})}$ , then the current gain  $\alpha$  would be  $\alpha_T$

## Base minority carrier transit time

$$\tau_t = \frac{W_B^2}{2D_h}$$

This **diffusion time** is the **transit time** of the minority carriers across the base

# BJT Common base dc characteristics

## Base transport factor

$$\alpha_T = \frac{I_C}{I_{E(\text{hole})}} = 1 - \frac{\tau_t}{\tau_h}$$

## CB current gain

$$\alpha = \alpha_T \gamma = \left( 1 - \frac{\tau_t}{\tau_h} \right) \gamma$$

# BJT Common base dc characteristics

## Base current

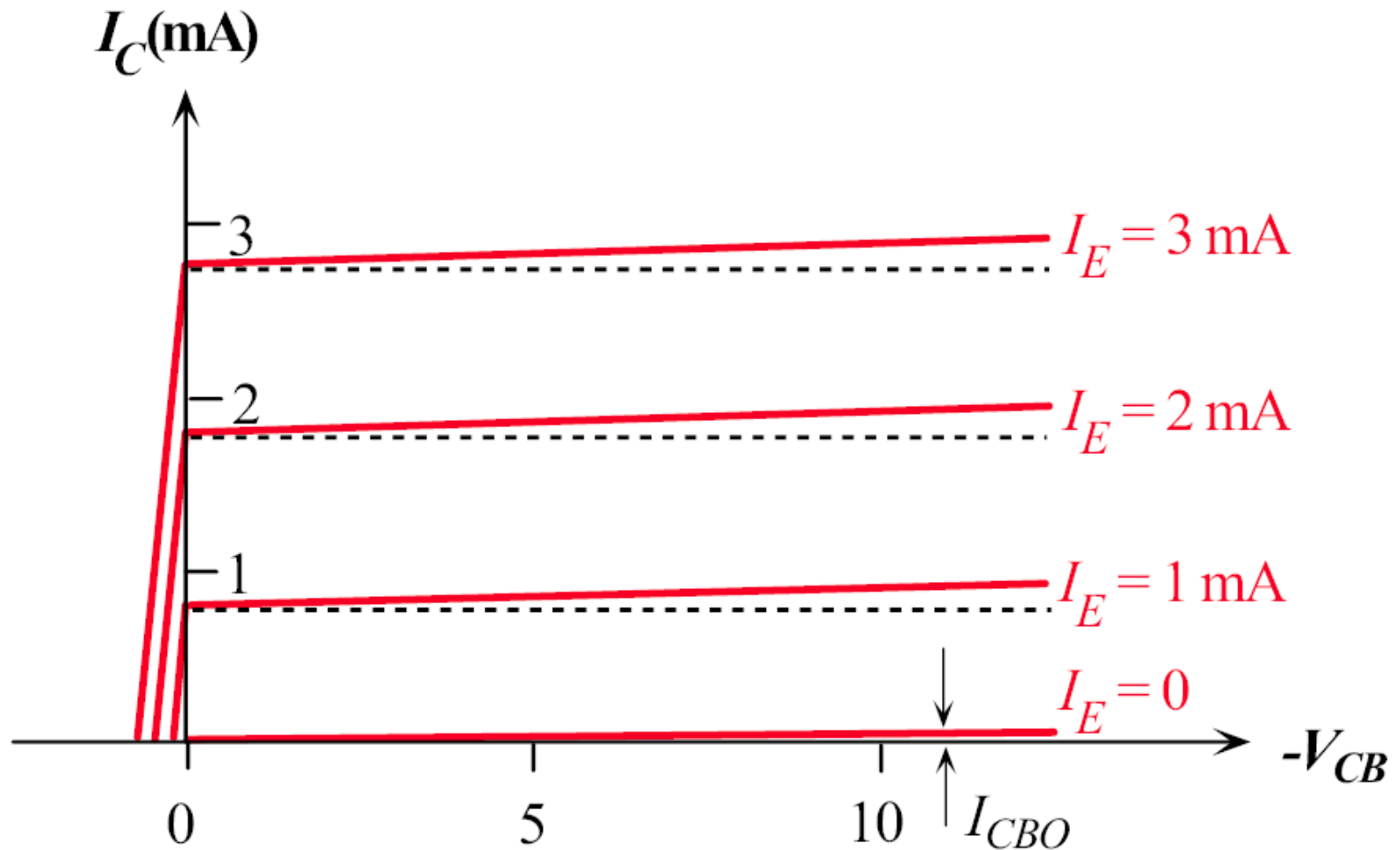
$$I_B = \left( \frac{\tau_t}{\tau_h} \right) I_{E(\text{hole})} + I_{E(\text{electron})} = \gamma \frac{\tau_t}{\tau_h} I_E + (-\gamma) I_E$$

or

$$I_B = I_E - I_C$$

## Base to collector current gain

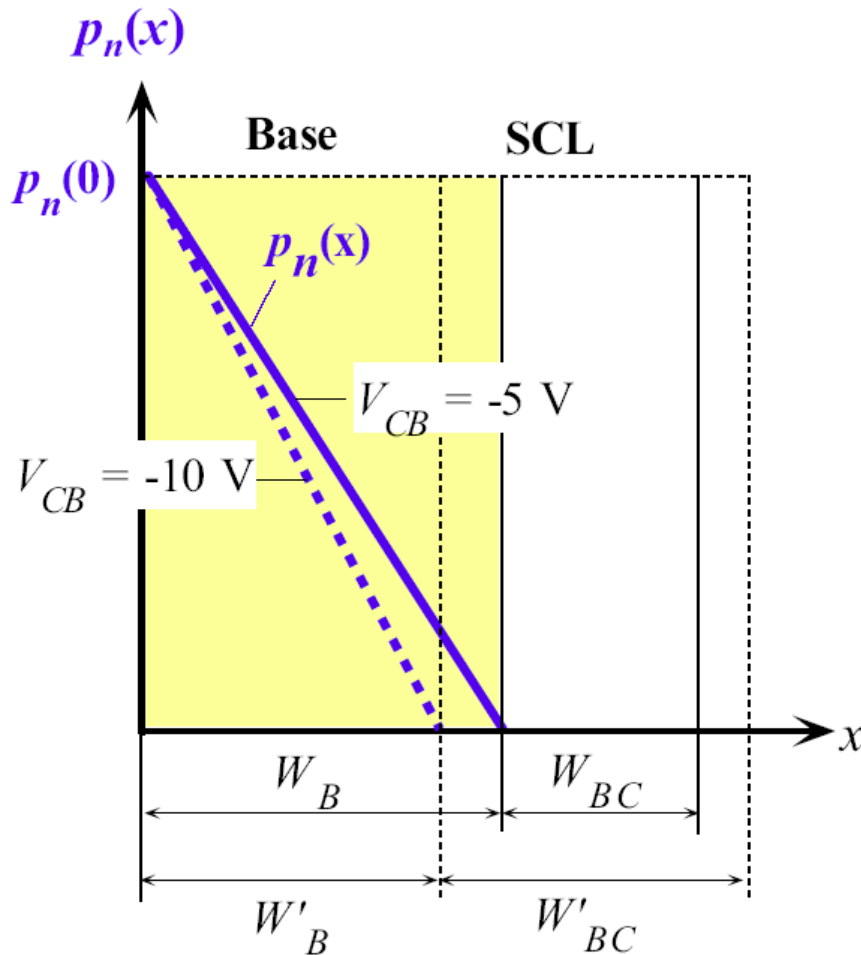
$$\beta = \frac{I_C}{I_B} = \frac{\alpha}{1 - \alpha} \approx \frac{\gamma \tau_h}{\tau_t}$$



DC  $I$ - $V$  characteristics of the pnp bipolar transistor (exaggerated to highlight various effects)

Fig 6.21

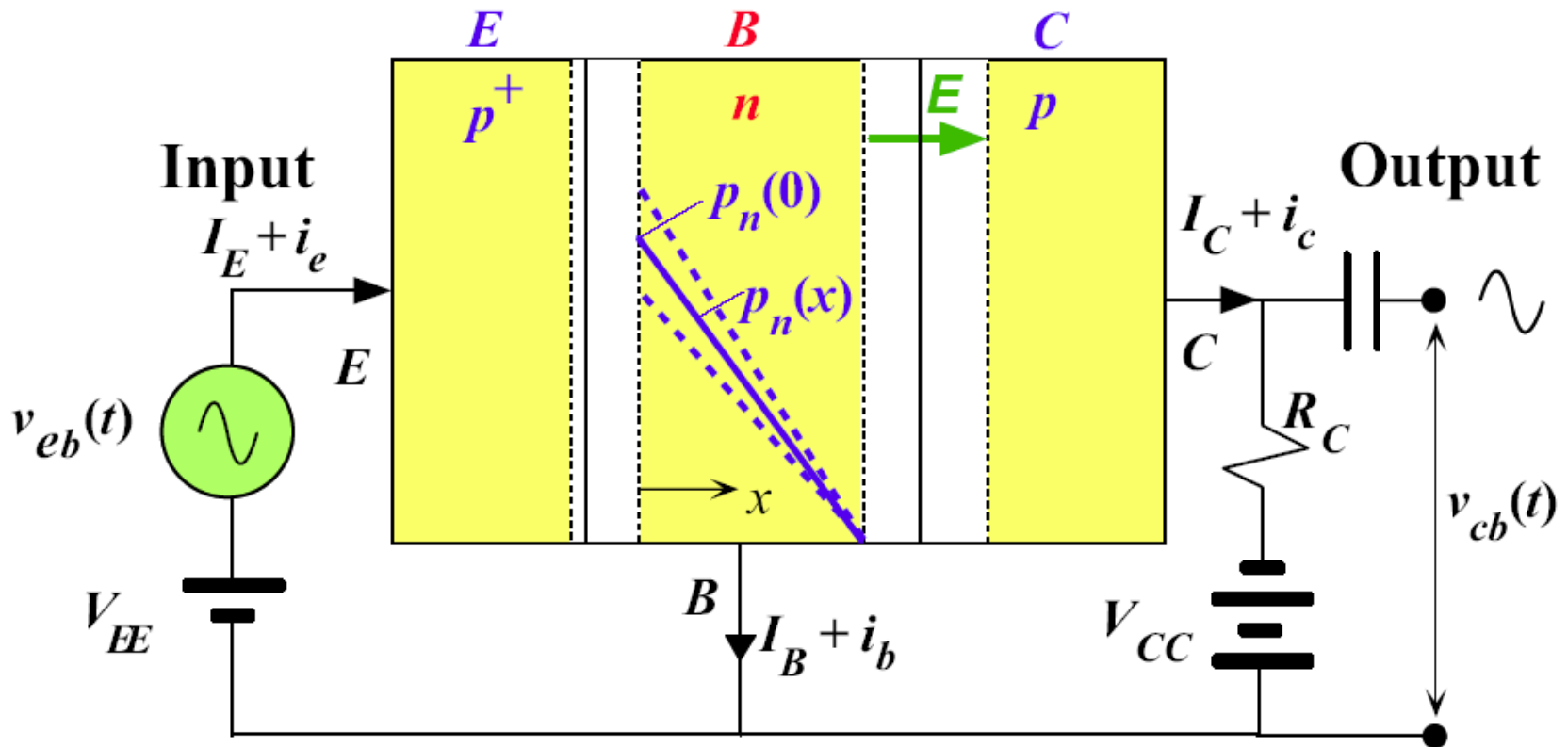
# The Early Effect



The Early effect. When the BC reverse bias increases, the depletion width  $W_{BC}$  increases to  $W'_{BC}$  which reduces the base width  $W_B$  to  $W'_B$ . As  $p_n(0)$  is constant (constant  $V_{EB}$ ), the minority carrier concentration gradient becomes steeper and the collector current  $I_C$  increases.

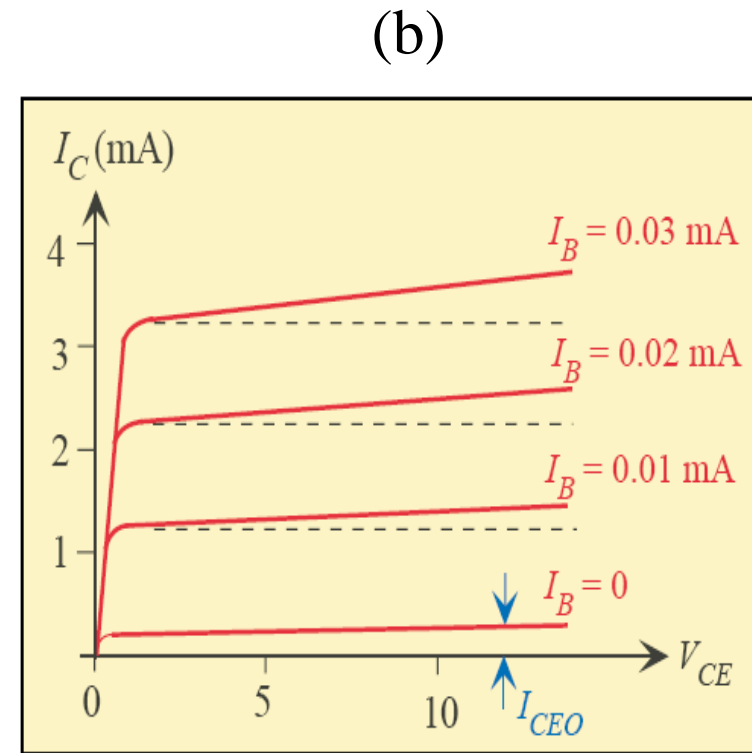
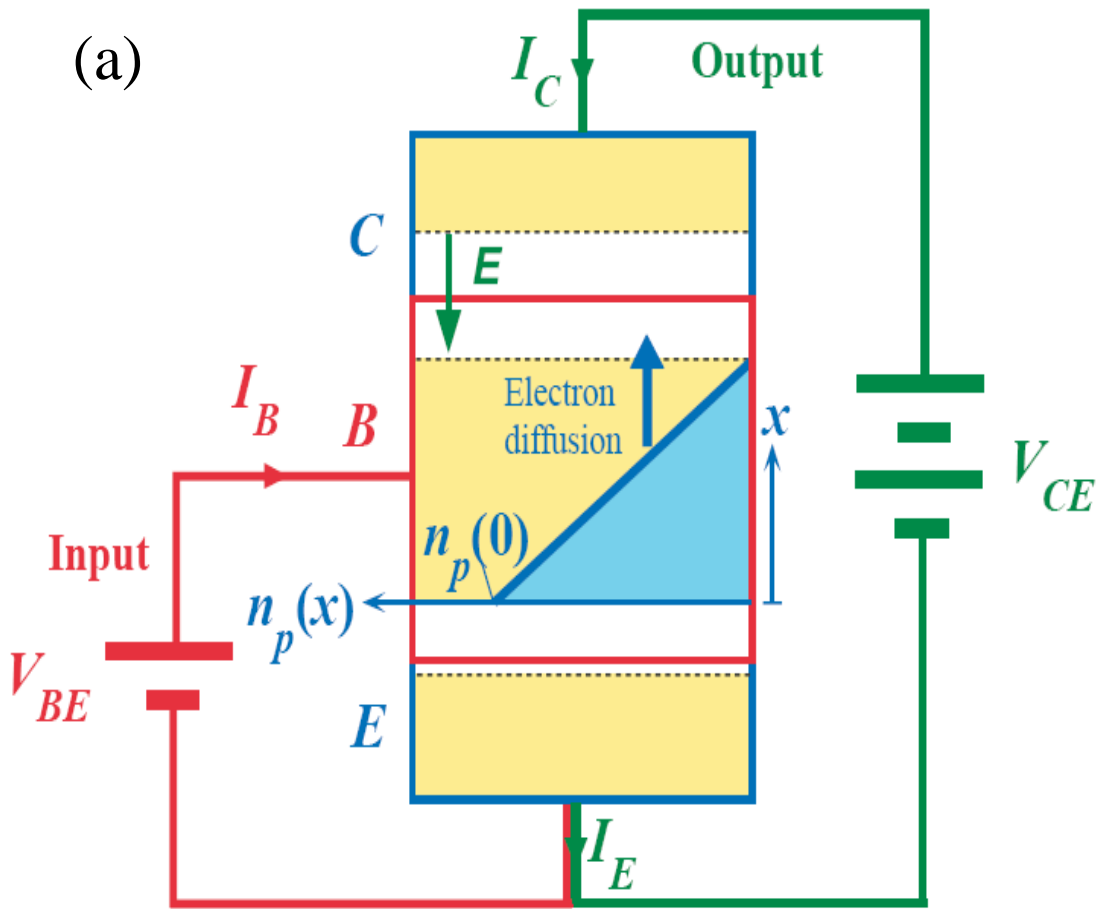
Fig 6.22





A *pnp* transistor operated in the active region in the common base amplifier configuration. The applied (input) signal  $v_{eb}$  modulates the dc voltage across the *BE* junction and hence modulates the injected hole concentration up and down about the dc value  $p_n(0)$ . The solid line shows how  $p_n(x)$  is modulated up and down by the signal  $v_{eb}$  superimposed on  $V_{EE}$ .

Fig 6.23



(a) An *npn* transistor operated in the active region in the common emitter (CE) configuration. The dc voltage across the BE junction,  $V_{BE}$ , controls the current  $I_E$  and hence  $I_B$  and  $I_C$ . The input current is the current that flows between  $V_{BE}$  and the base which is  $I_B$ . The output current is the current flowing between  $V_{CE}$  and the collector which is  $I_C$ .

(b) DC  $I$ - $V$  characteristics of the *npn* bipolar transistor in the CE configuration (exaggerated to highlight various effects).

# Common Emitter dc characteristics

Active region collector current

$$I_C = \beta I_B + I_{CEO}$$

where

$$I_{CEO} = \frac{I_{CBO}}{(-\alpha)} \approx \beta I_{CBO}$$

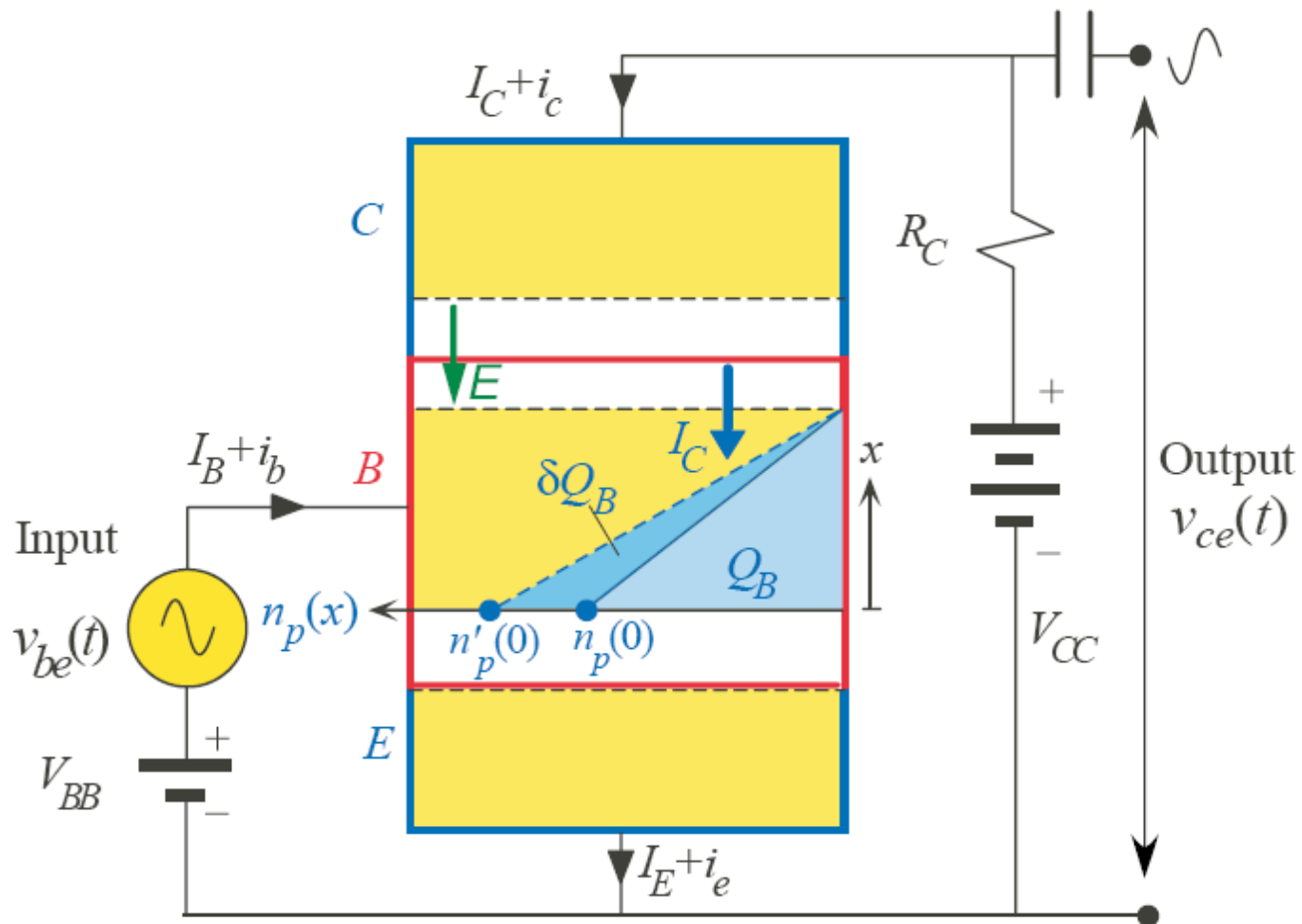
# Common Base Amplifier

Small signal input resistance

$$r_e = \frac{\delta V_{EB}}{\delta I_E} = \frac{kT}{eI_E} = \frac{25}{I_E (\text{mA})}$$

CB voltage gain (small signal)

$$A_V = \frac{v_{cb}}{v_{eb}} = \frac{R_C}{r_e}$$



An *npn* transistor operated in the active region in the common emitter amplifier configuration. The applied signal  $v_{be}$  modulates the dc voltage across the BE junction and hence modulates the injected minority concentration up and down about the dc value  $n_p(0)$ . The solid line shows  $n_p(x)$  when only the dc bias  $V_{BB}$  is present. The dashed line shows how  $n_p(x)$  is modulated up by a positive small signal  $v_{be}$  superimposed on  $V_{BB}$ .

Fig 6.25

# Common Emitter dc characteristics

## Emitter current and $V_{BE}$

$$I_E = I_{EO} \exp\left(\frac{eV_{BE}}{kT}\right)$$

where  $I_{EO}$  is a constant

## Input resistance (small signal)

$$r_{be} = \frac{v_{be}}{i_b} = \frac{\delta V_{BE}}{\delta I_B} \approx \beta \frac{\delta V_{BE}}{\delta I_E} \approx \frac{\beta 25}{I_C (\text{mA})}$$

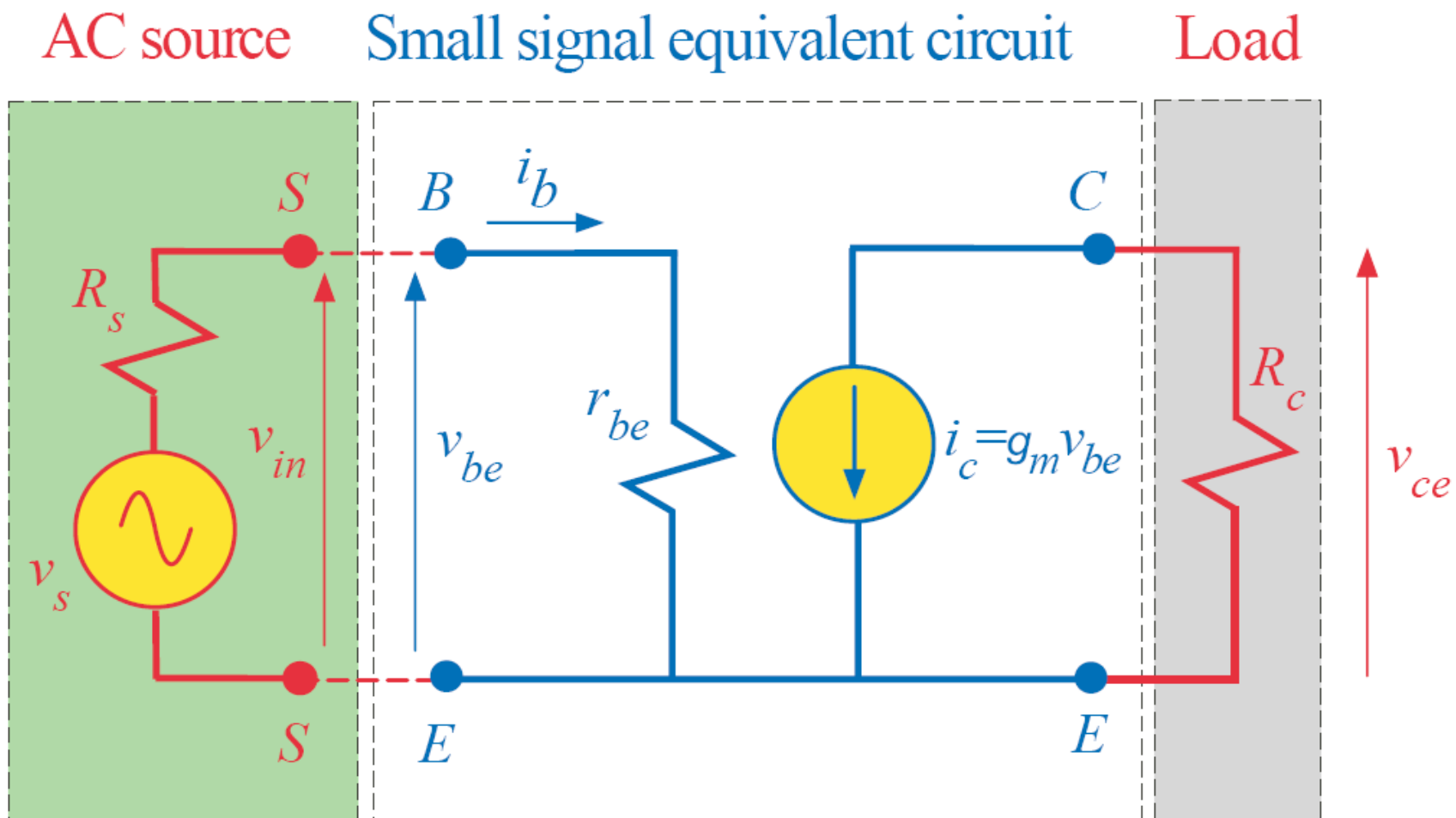
# Common Emitter dc characteristics

Transconductance,  $g_m$

$$g_m = \frac{i_c}{v_{be}} \approx \frac{\delta I_E}{\delta V_{BE}} = \frac{I_E (\text{mA})}{25} = \frac{1}{r_e}$$

Voltage gain

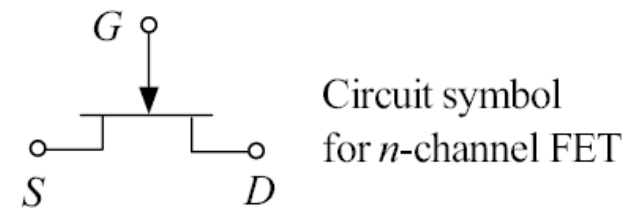
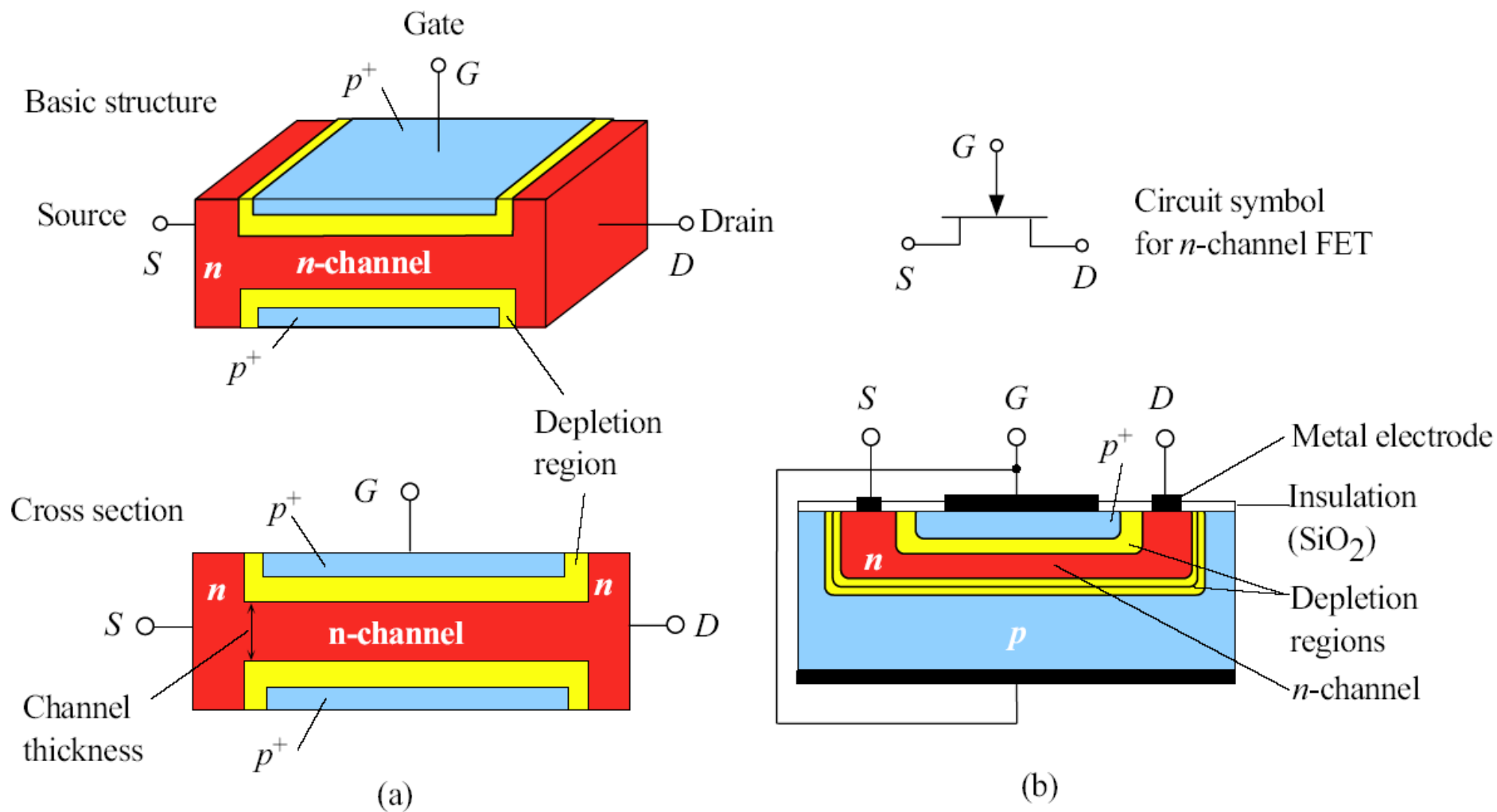
$$A_V = -g_m R_C$$



Low frequency small signal simplified equivalent circuit of the bipolar transistor in the CE configuration with a load resistor  $R_C$  in the collector circuit.

Fig 6.26





2N5461  
2N5462

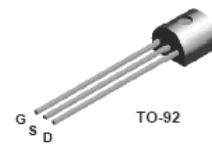
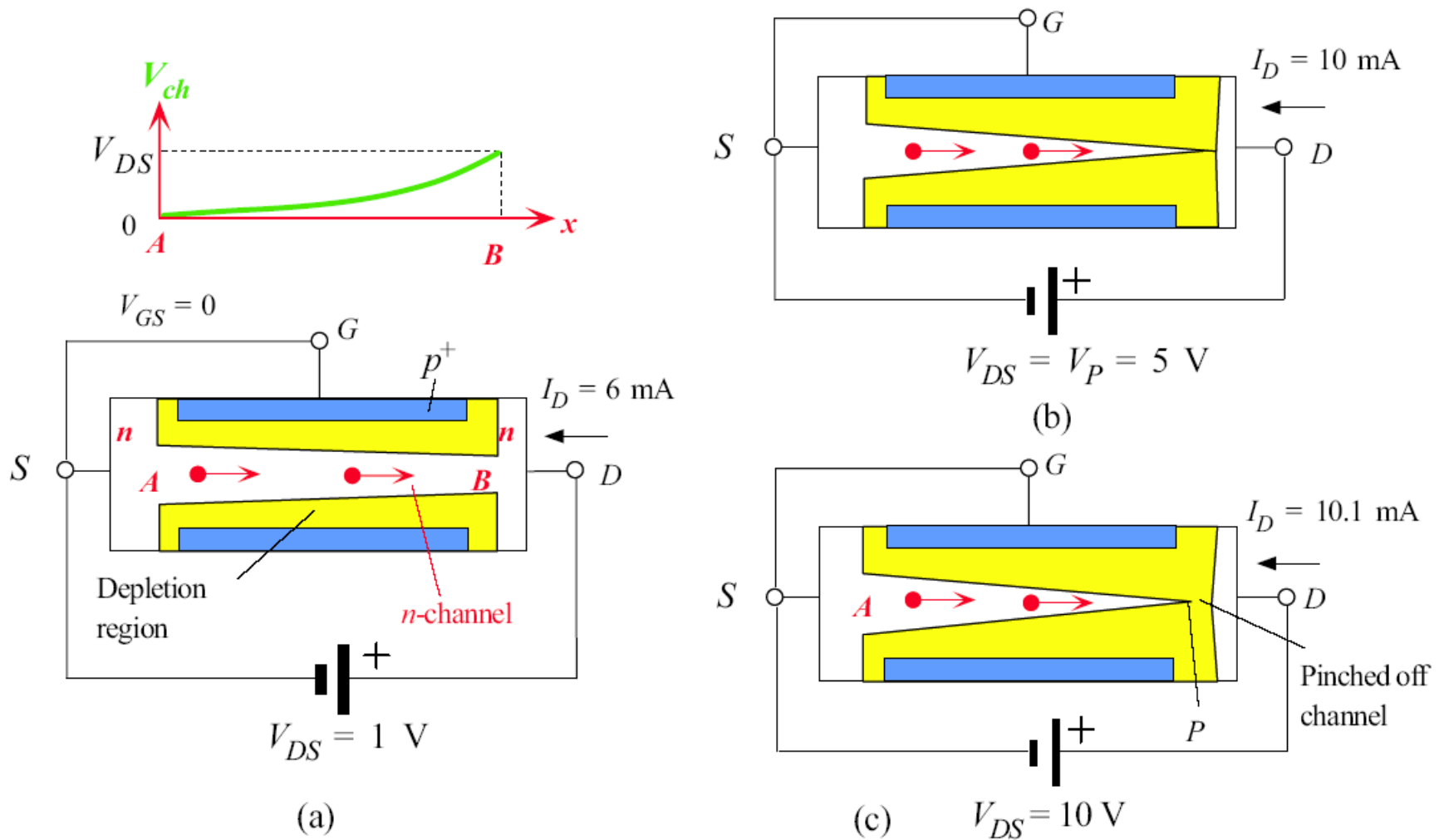
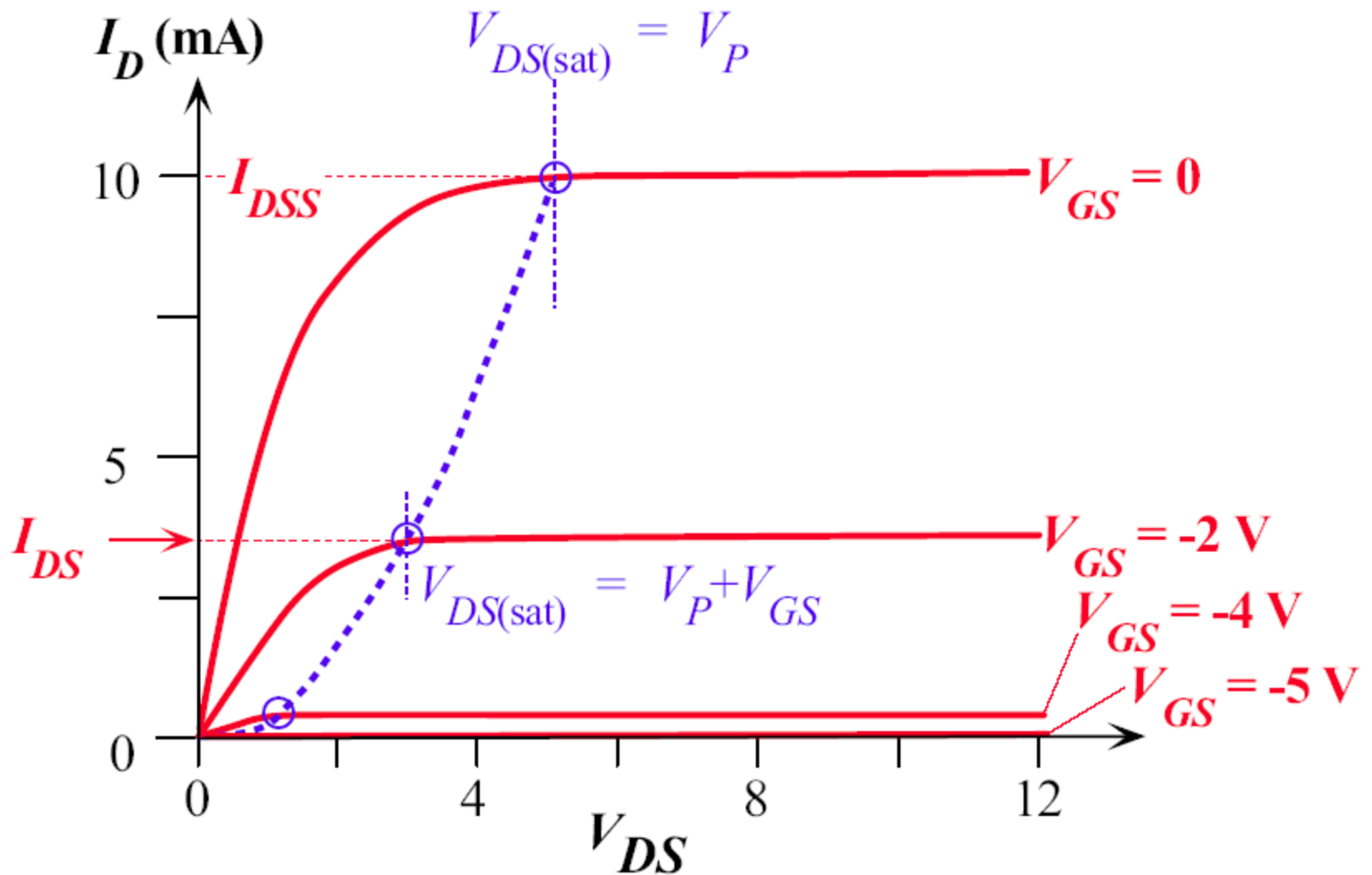


Fig 6.27



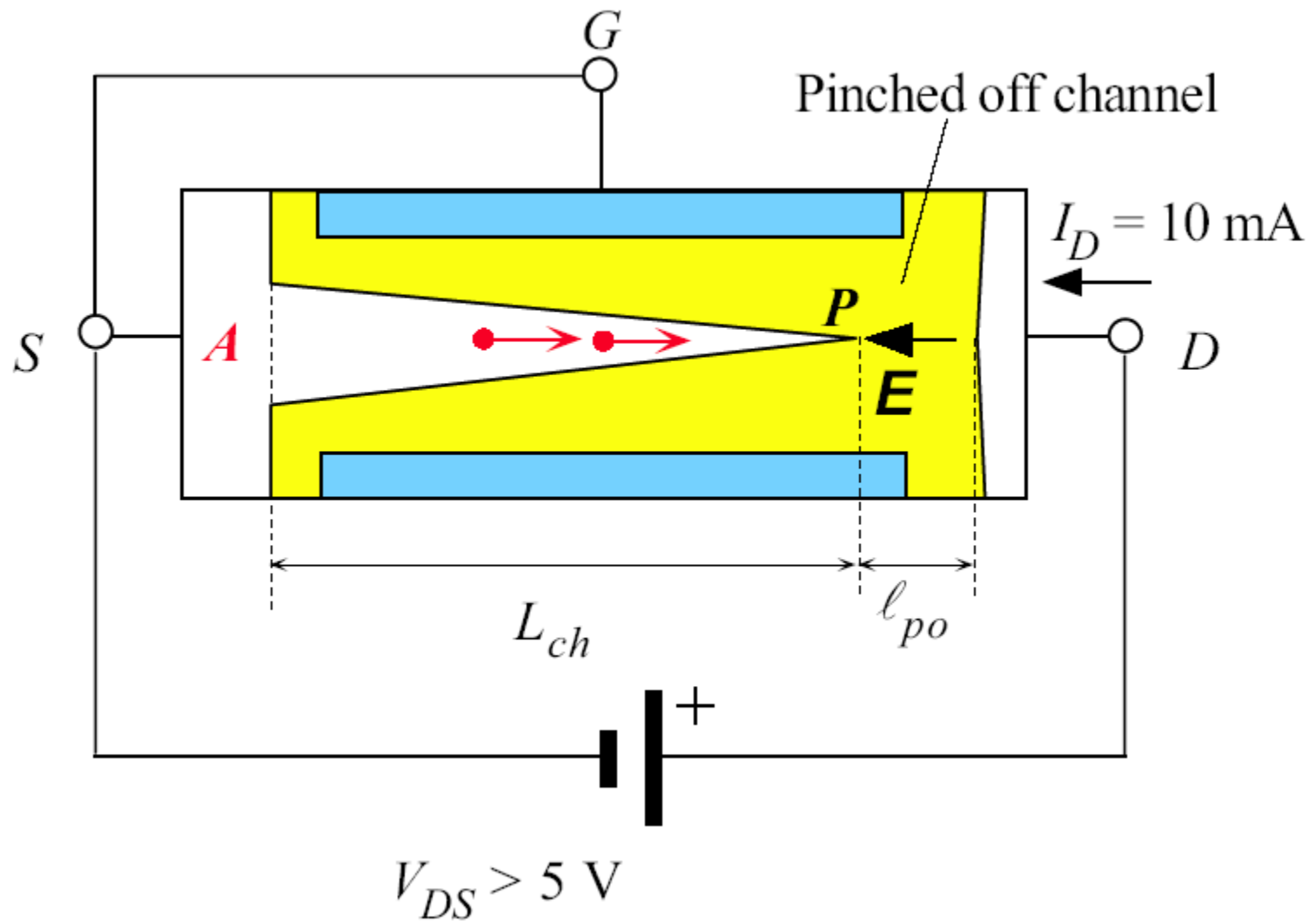
- (a) The gate and source are shorted ( $V_{GS} = 0$ ) and  $V_{DS}$  is small,  
 (b)  $V_{DS}$  has increased to a value that allows the two depletion layers to just touch, when  $V_{DS} = V_P (= 5 \text{ V})$  when the  $p^+n$  junction voltage at the drain end,  $V_{GD} = -V_{DS} = -V_P = -5 \text{ V}$ .  
 (c)  $V_{DS}$  is large ( $V_{DS} > V_P$ ) so that a short length of the channel is pinched off.

Fig 6.28



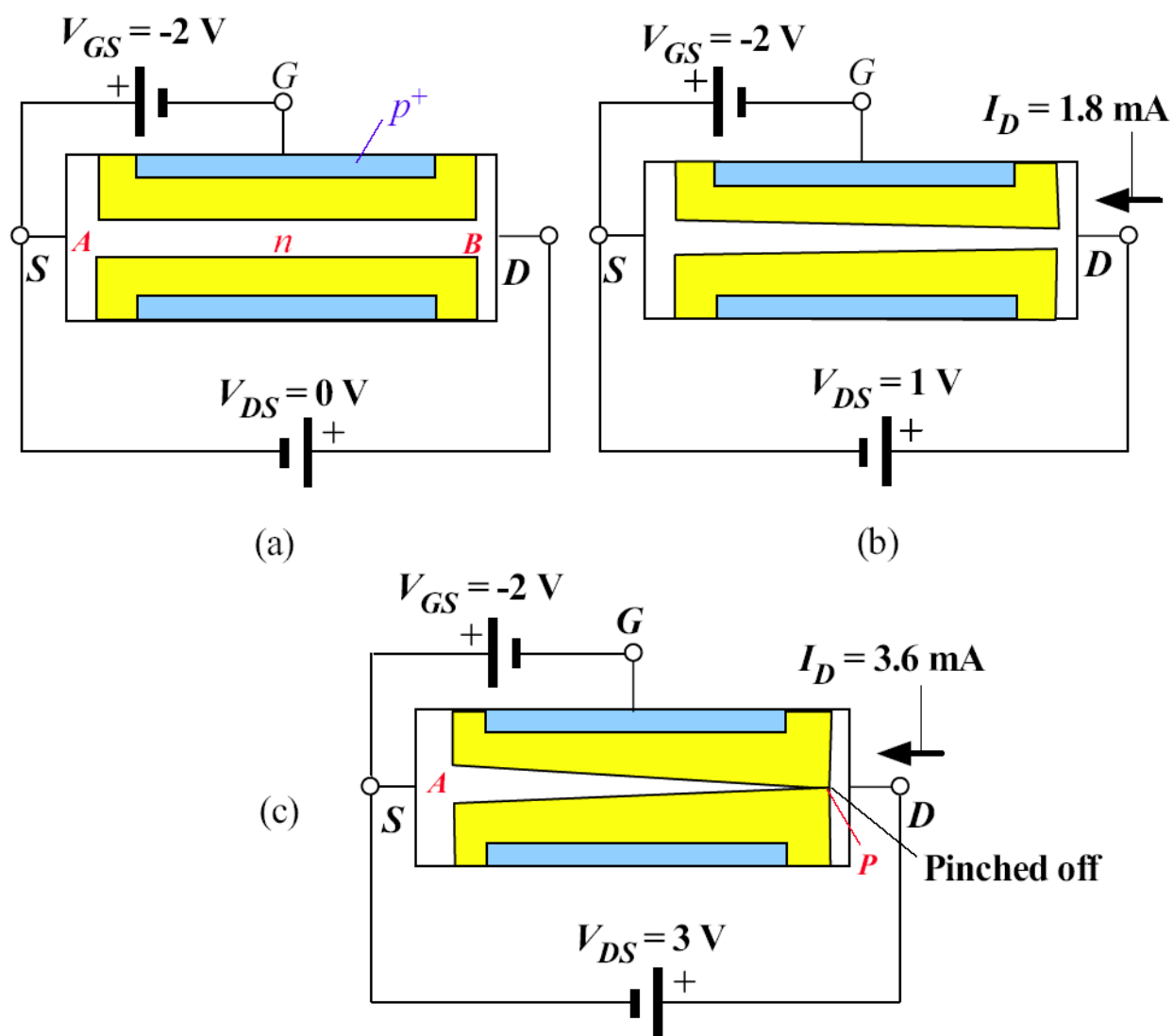
Typical  $I_D$  vs.  $V_{DS}$  characteristics of a JFET for various fixed gate voltages  $V_{GS}$ .

Fig 6.29



The pinched-off channel and conduction for  $V_{DS} > V_P (=5 \text{ V})$

Fig 6.30



(a) The JFET with a negative  $V_{GS}$  voltage has a narrower  $n$ -channel at the start. (b) Compared to the  $V_{GS} = 0$  case, the same  $V_{DS}$  gives less  $I_D$  as the channel is narrower. (c) The channel is pinched off at  $V_{DS} = 3\text{ V}$  sooner than the  $V_{GS} = 0$  case where it was  $V_{DS} = 5\text{ V}$ .

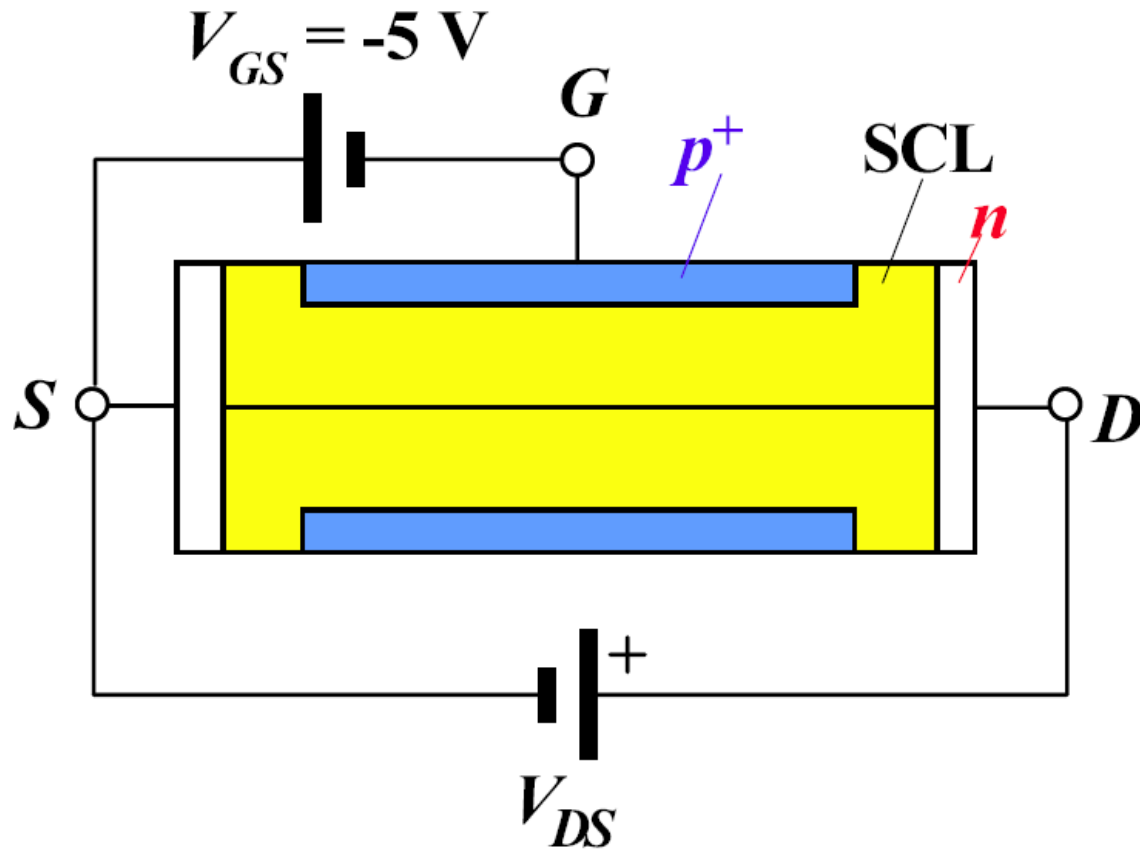
Fig 6.31

# Junction field effect transistor (JFET)

## Pinch-off condition

$$V_{DS(\text{sat})} = V_P + V_{GS}$$

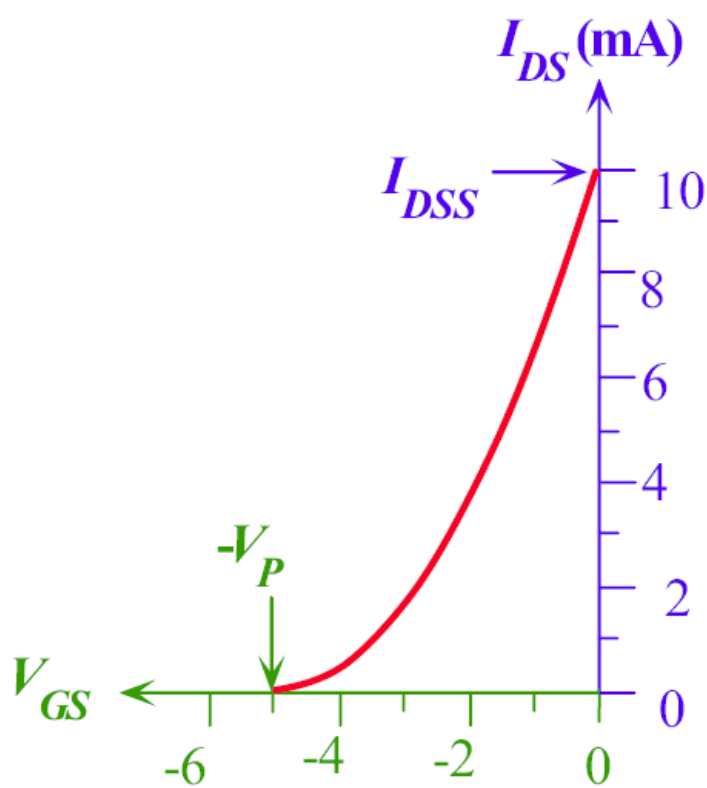
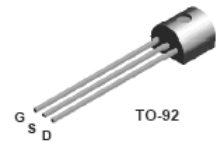
where  $V_{GS}$  is a negative voltage (reducing  $V_P$ ). Beyond pinch-off when  $V_{DS} > V_{DS(\text{sat})}$ , the point  $P$  where the channel is just pinched still remains at potential  $V_{DS(\text{sat})}$ , given by the above equation.



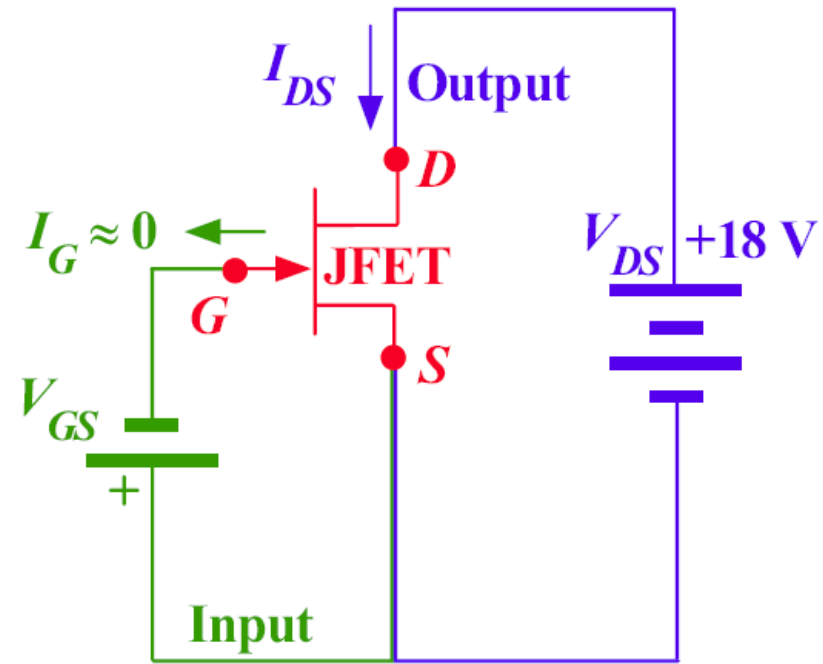
When  $V_{GS} = -5\text{ V}$  the depletion layers close the whole channel from the start, at  $V_{DS} = 0$ . As  $V_{DS}$  is increased there is a very small drain current which is the small reverse leakage current due to thermal generation of carriers in the depletion layers.

Fig 6.32

2N5460  
2N5461  
2N5462



(a)



(b)

(a) Typical  $I_{DS}$  versus  $V_{GS}$  characteristics of a JFET. (b) The dc circuit where  $V_{GS}$  in the gate–source circuit (input) controls the drain current  $I_{DS}$  in the drain–source (output) circuit in which  $V_{DS}$  is kept constant and large ( $V_{DS} > V_P$ ).

Fig 6.33



# Junction field effect transistor (JFET)

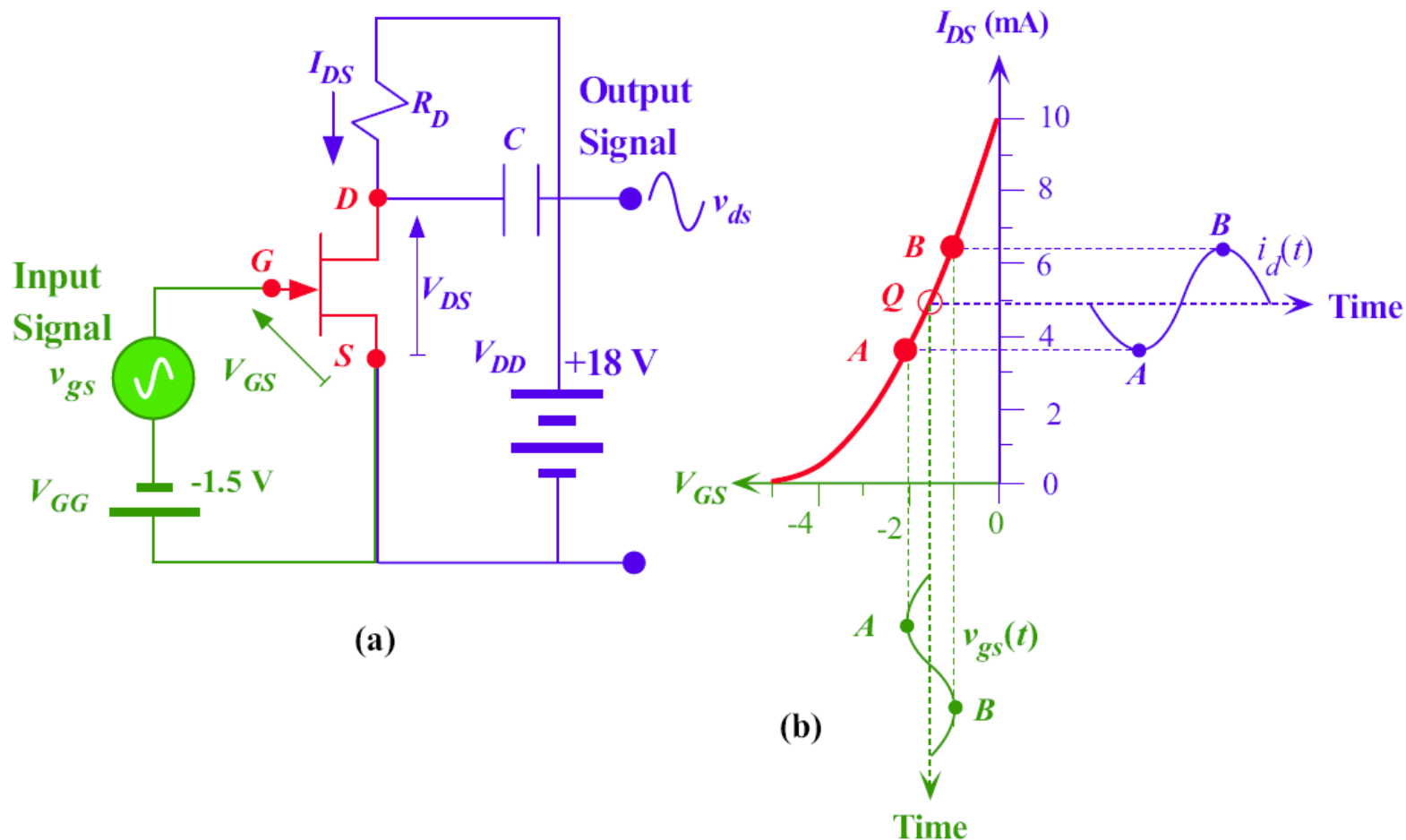
## Beyond pinch-off

$$I_{DS} = I_{DSS} \left[ 1 - \left( \frac{V_{GS}}{V_{GS(\text{off})}} \right) \right]^2$$

where,

$I_{DSS}$  is the drain current when  $V_{GS} = 0$

$V_{GS(\text{off})} = -V_p$ ; the gate-source voltage that just pinches off the channel



(a)

(b)

- (a) Common source (CS) ac amplifier using a JFET.
- (b) Explanation of how  $I_D$  is modulated by the signal  $v_{gs}$  in series with the dc bias voltage  $V_{GG}$ .

Fig 6.34

**Table 6.1** Voltage and current in the common source amplifier of Figure 6.34a

$v_{gs}$ (V)	$V_{GS}$ (V)	$I_{DS}$ (mA)	$i_d$ (mA)	$V_{DS} = V_{DD} - I_{DS}R_D$	$v_{ds}$ (V)	Voltage Gain	Comment
0	-1.5	4.9	0	8.2	0		dc conditions, point $Q$
-0.5	-2.0	3.6	-1.3	10.8	+2.6	-5.2	Point A
+0.5	-1.0	6.4	+1.5	5.2	-3.0	-6	Point B

# JFET Amplifier

## Definition of the JFET transconductance (small signal)

$$g_m = \frac{dI_{DS}}{dV_{GS}} \approx \frac{\delta I_{DS}}{\delta V_{GS}} = \frac{i_d}{v_{gs}}$$

## JFET transconductance (small signal)

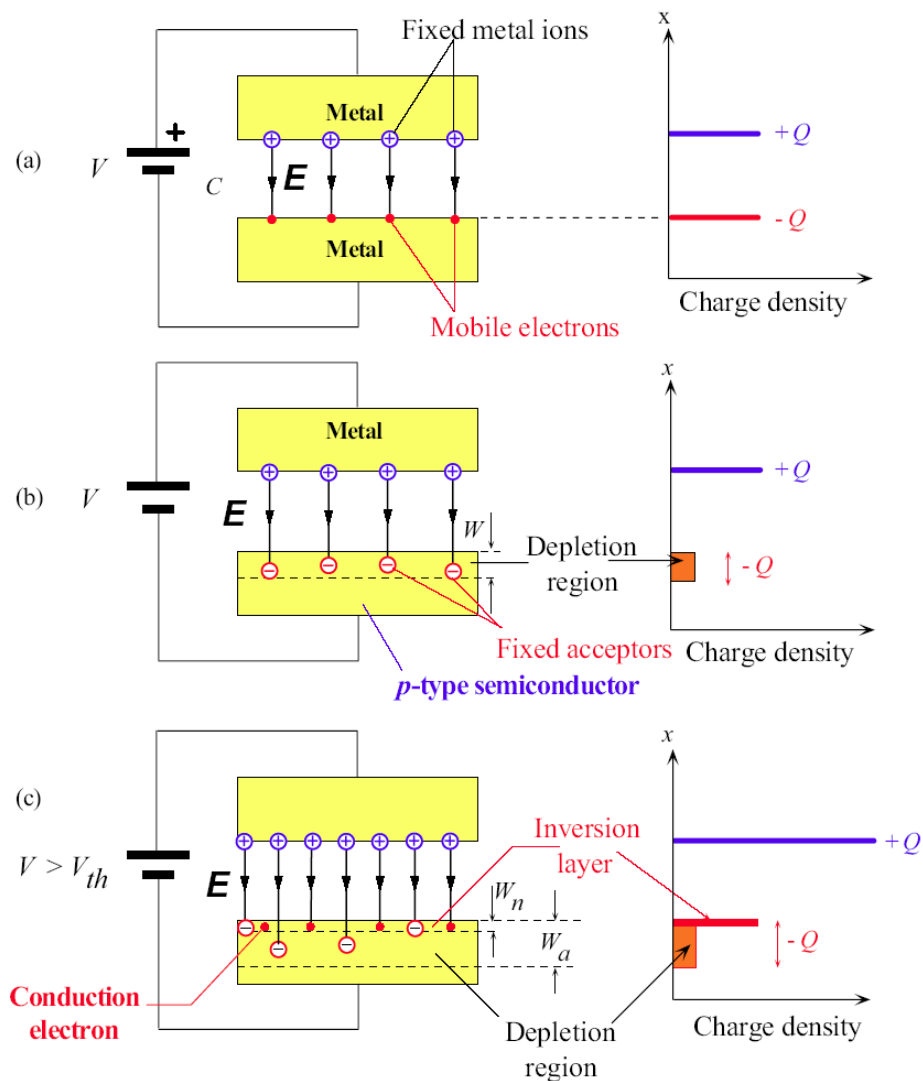
$$g_m = \frac{dI_{DS}}{dV_{GS}} = -\frac{2I_{DSS}}{V_{GS(off)}} \left[ 1 - \left( \frac{V_{GS}}{V_{GS(off)}} \right) \right] = \frac{2 \left[ I_{DSS} I_{DS} \right]^{1/2}}{V_{GS(off)}}$$

# JFET Amplifier

Small-signal voltage gain

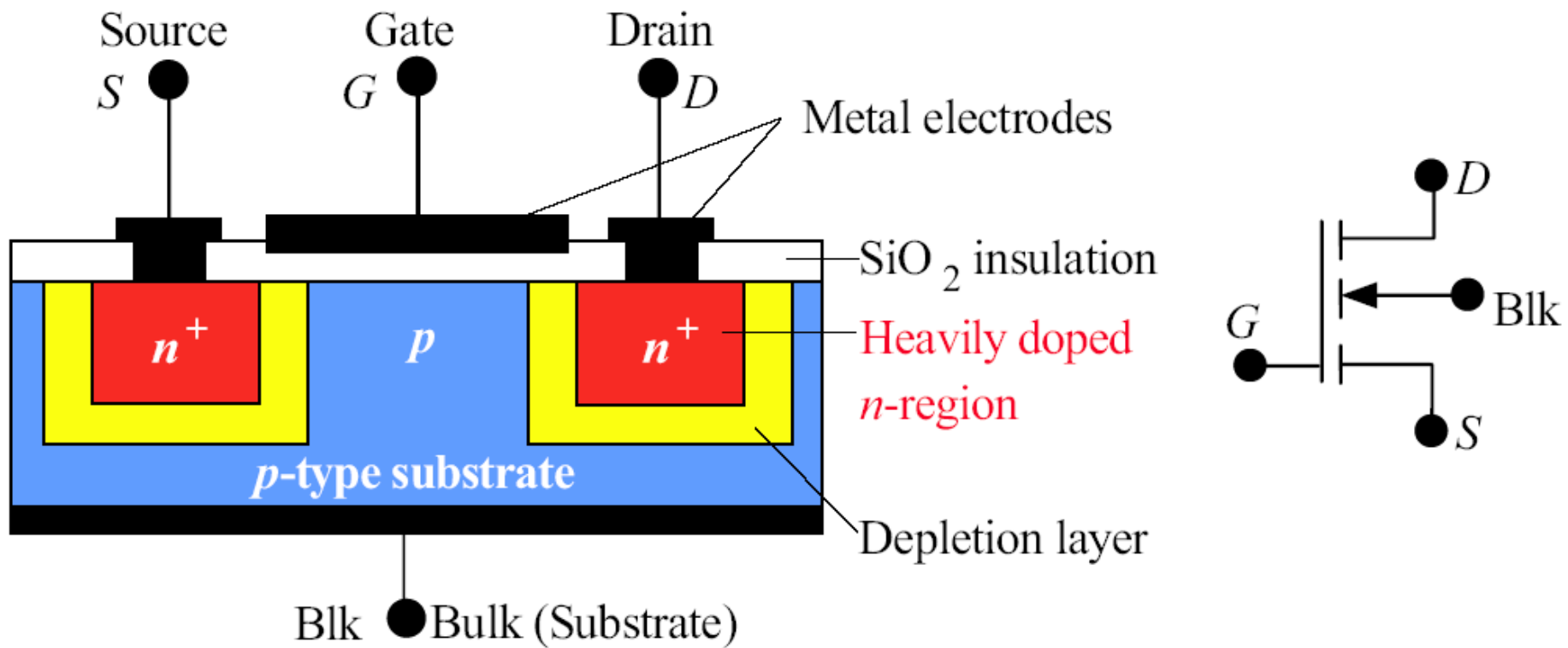
$$A_V = \frac{v_{ds}}{v_{gs}} = \frac{-R_D i_d}{v_{gs}}$$

$$A_V = \frac{-R_D (g_m v_{gs})}{v_{gs}} = -g_m R_D$$



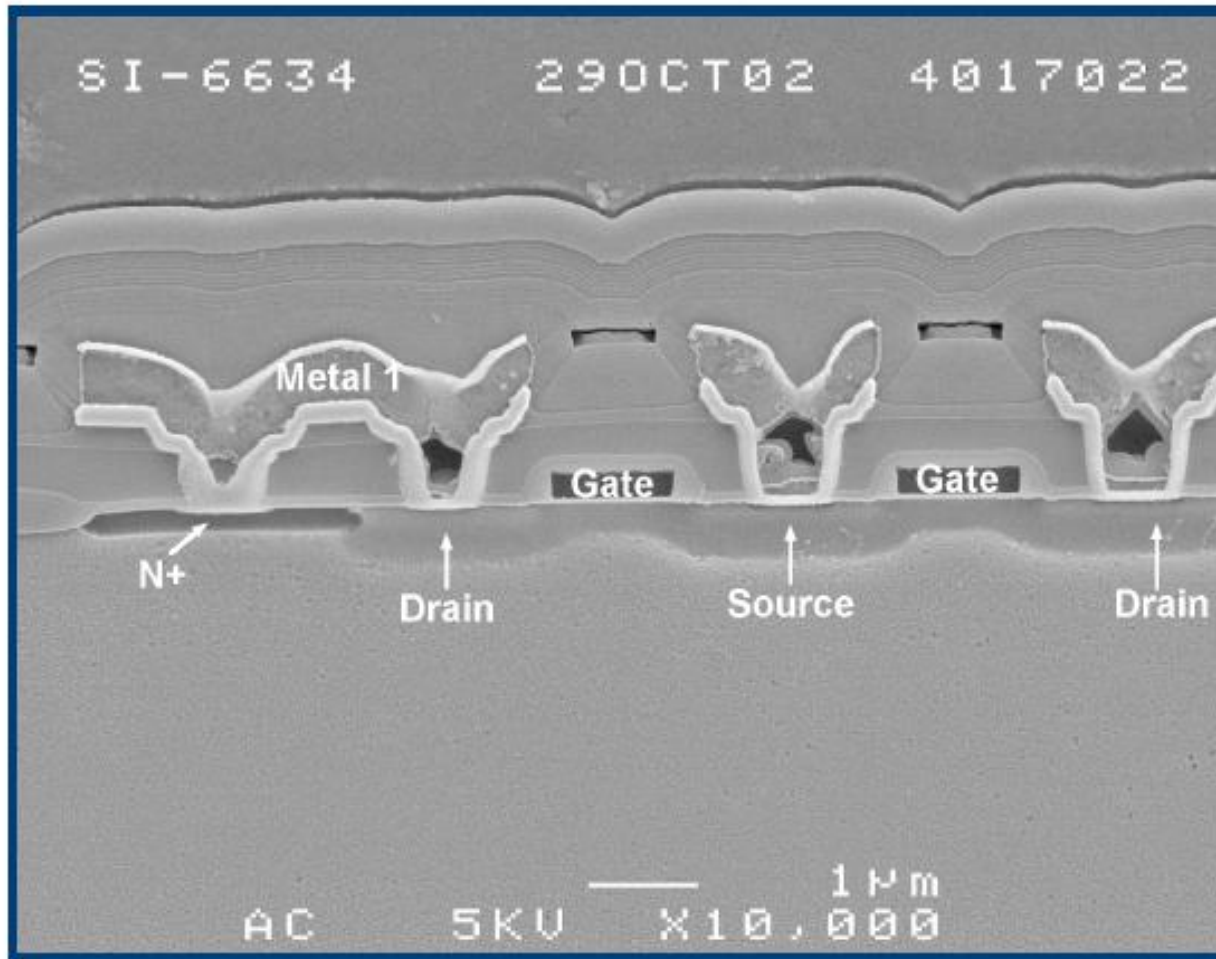
The field effect. (a) In a metal-air-metal capacitor, all the charges reside on the surface. (b) Illustration of field penetration into a  $p$ -type semiconductor. (c) As the field increases eventually when  $V > V_{th}$  an inversion layer is created near the surface in which there are conduction electrons.

Fig 6.35



The basic structure of the enhancement MOSFET and its circuit symbol.

Fig 6.36

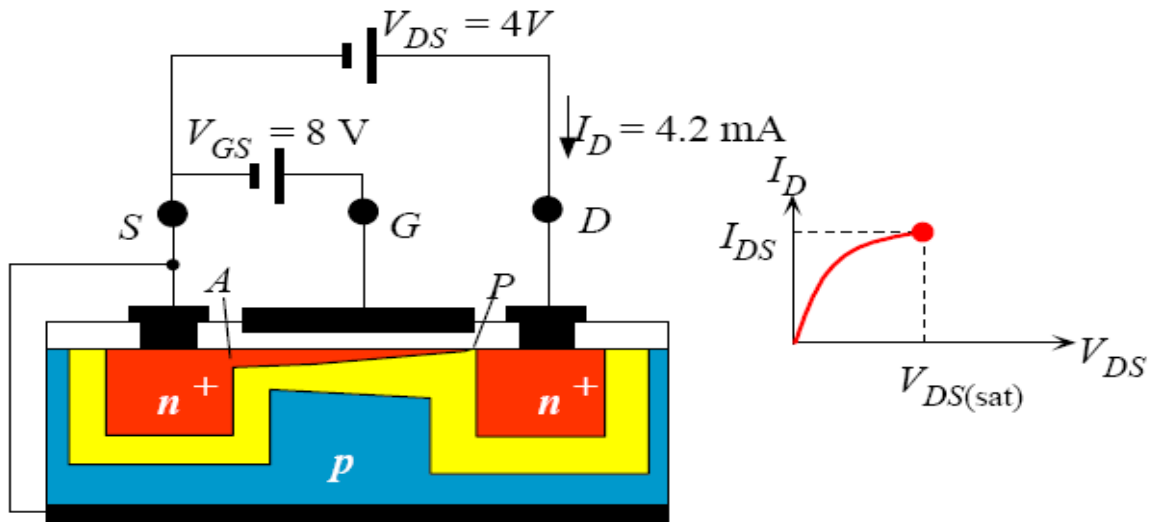


## SEM cross section of a MOS Transistor

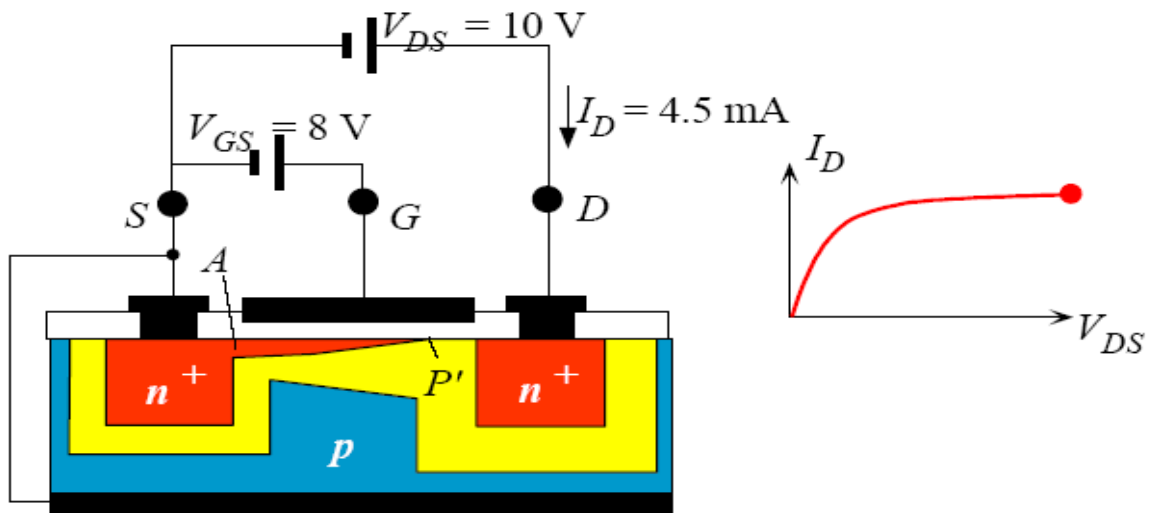
[SOURCE: Courtesy of Don Scansen, Semiconductor Insights, Kanata, Ontario, Canada]







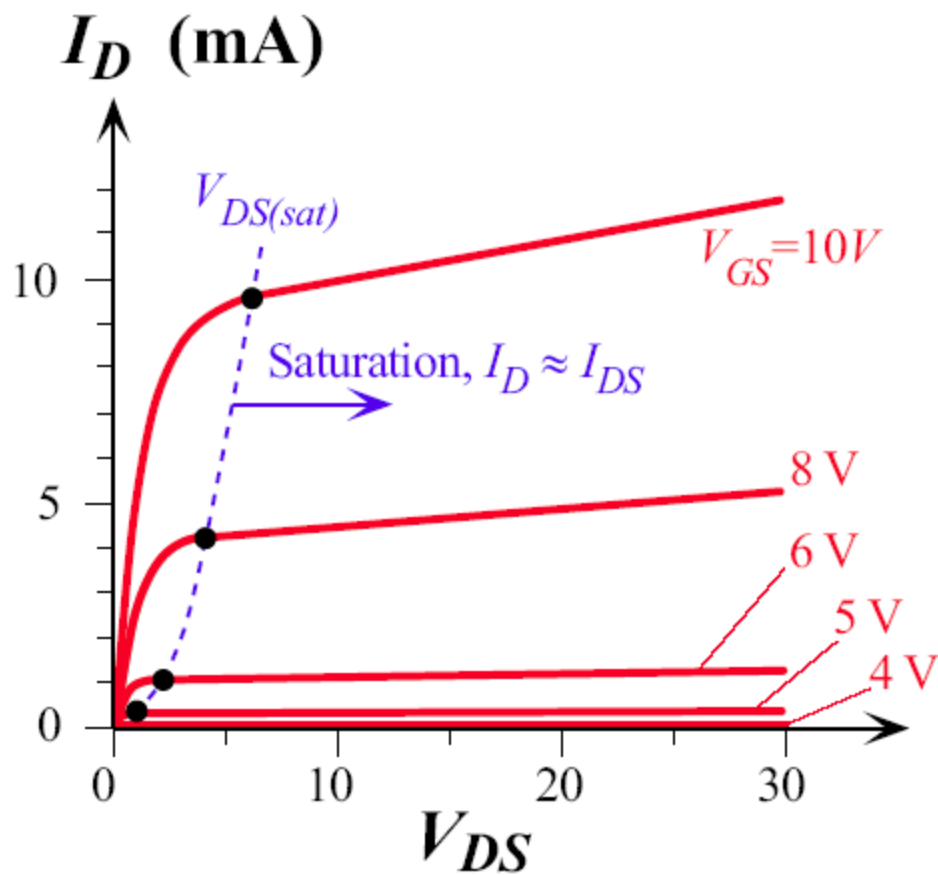
(c) Above threshold  $V_{GS} > V_{th}$  and saturation,  $V_{DS} = V_{DS(sat)}$



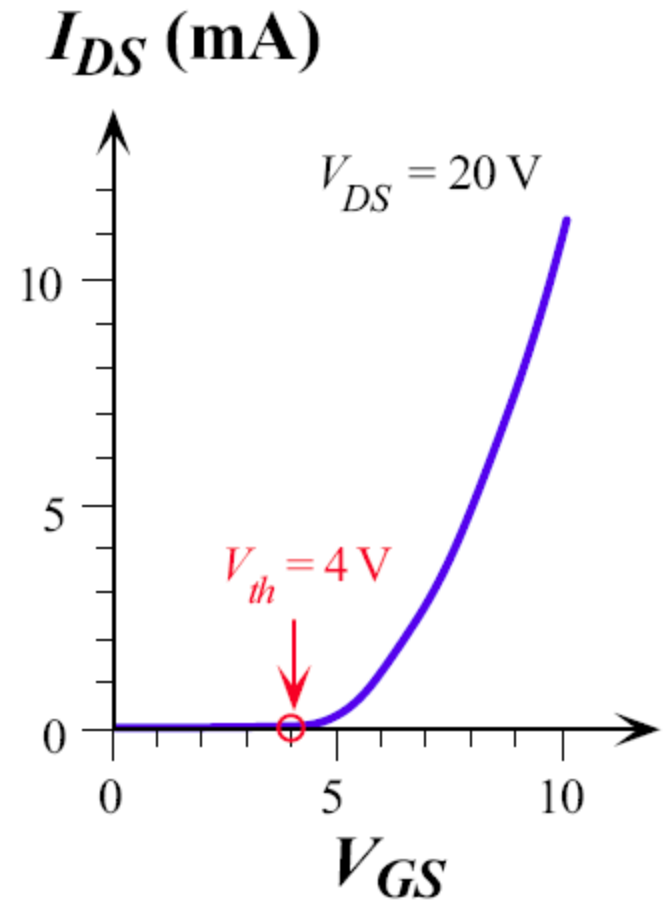
(d) Above threshold  $V_{GS} > V_{th}$  and saturation region,  $V_{DS} > V_{DS(sat)}$

The MOSFET  $I_D$  vs.  $V_{DS}$  characteristics

Fig 6.37



(a)



(b)

(a) Typical  $I_D$  vs  $V_{DS}$  characteristics of an enhancement MOSFET ( $V_{th} = 4$  V) for various Fixed voltages  $V_{GS}$ .

(b) Dependence of  $I_D$  on  $V_{GS}$  at a given  $V_{DS} (> V_{DS(sat)})$

Fig 6.38

# Enhancement NMOSFET

Enhancement NMOSFET constant

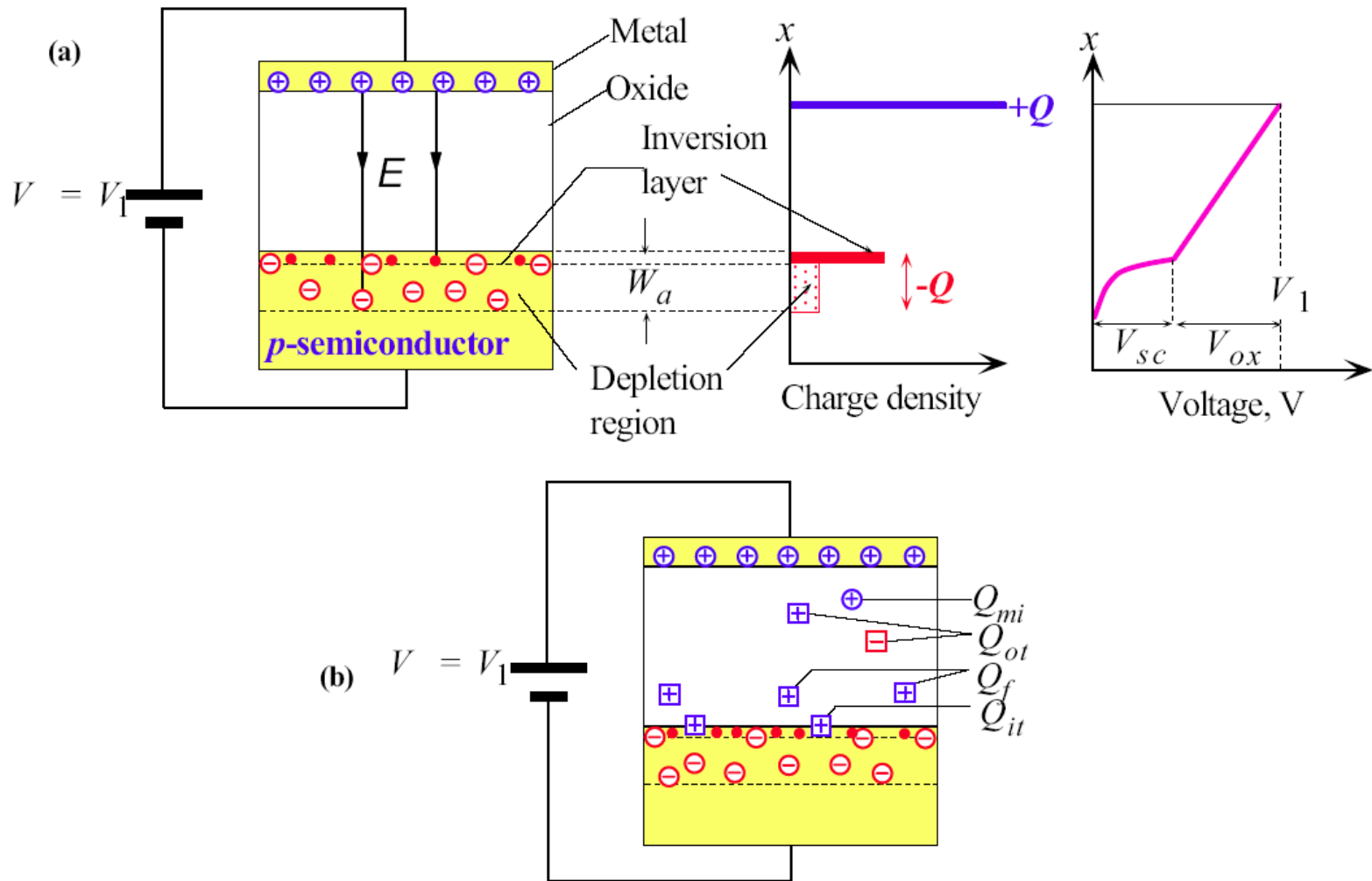
$$K = \frac{Z\mu_e\epsilon}{2Lt_{\text{ox}}}$$

where  $\mu_e$  is the electron drift mobility in the channel,  $L$  and  $Z$  are the length and width of the gate controlling the channel, and  $\epsilon$  and  $t_{\text{ox}}$  are the permittivity ( $\epsilon_r\epsilon_o$ ) and thickness of the oxide insulation under the gate

Enhancement MOSFET

$$I_{DS} = K \left( V_{GS} - V_{th} \right)^2 \left( 1 + \lambda V_{DS} \right)$$

Where  $\lambda$  is a constant that is typically  $0.01 \text{ V}^{-1}$ .

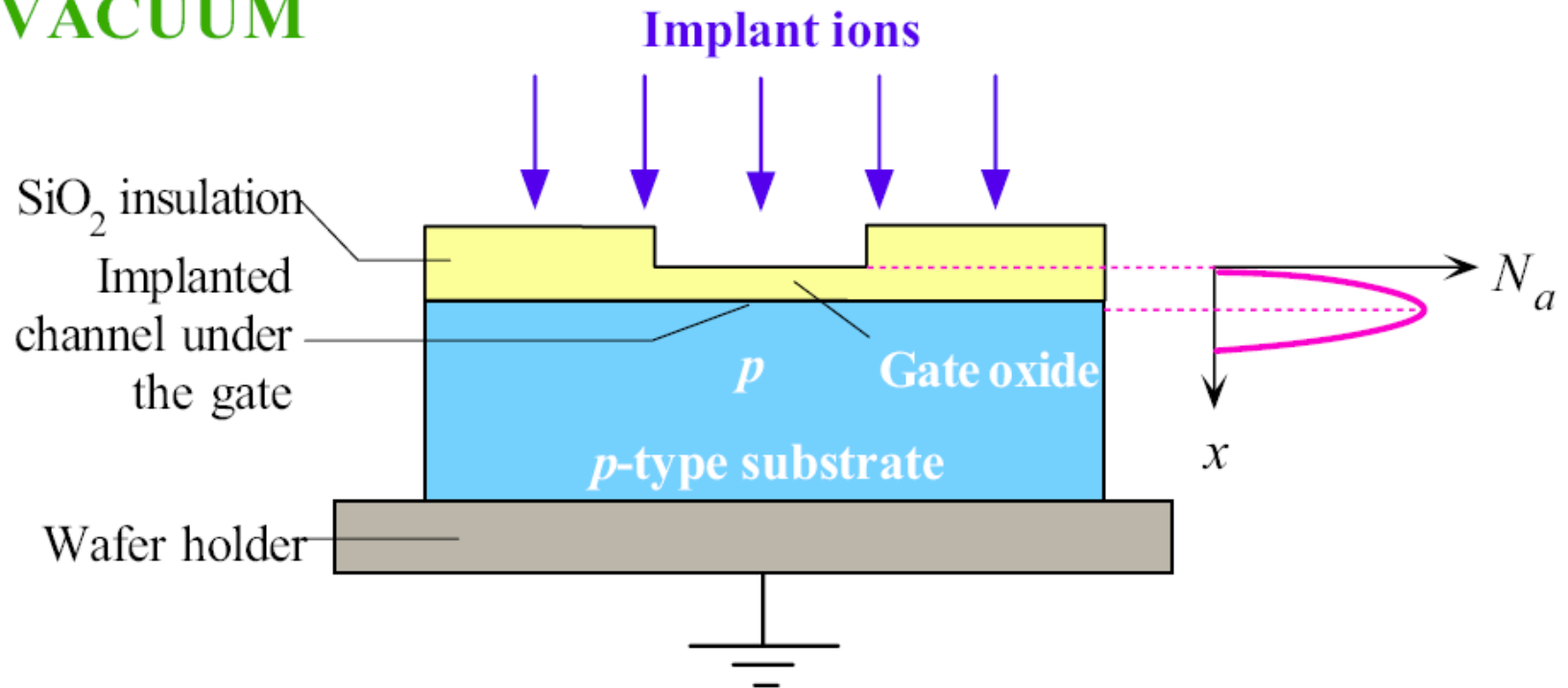


(a) The threshold voltage and the ideal MOS structure.

(b) In practice, there are several charges in the oxide and at the oxide-semiconductor interface that effect the threshold voltage:  $Q_{mi}$  = Mobile ionic charge (e.g.  $\text{Na}^+$ ),  $Q_{ot}$  = Trapped oxide charge,  $Q_f$  = Fixed oxide charge,  $Q_{it}$  = Charge trapped at the interface.

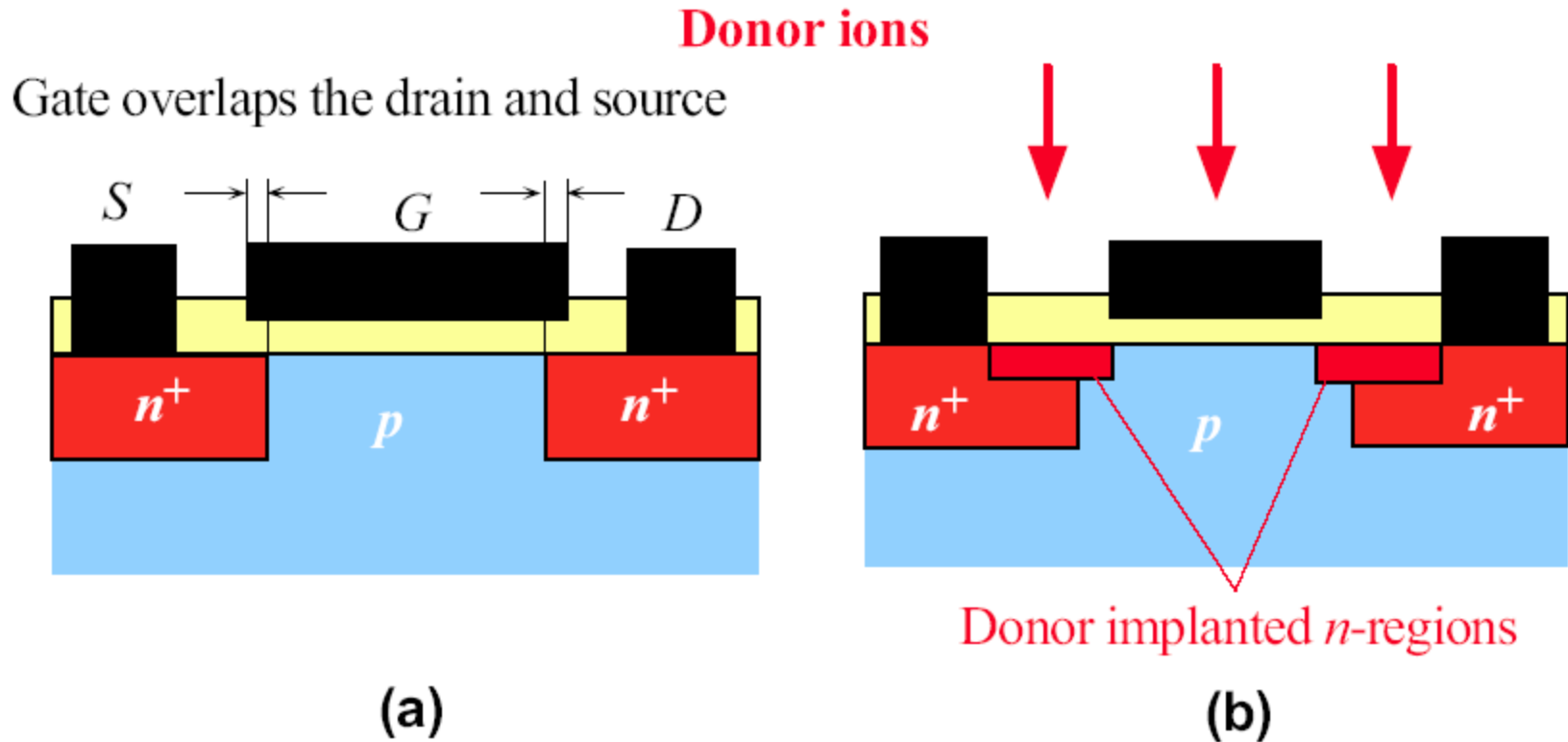
Fig 6.39

**VACUUM**



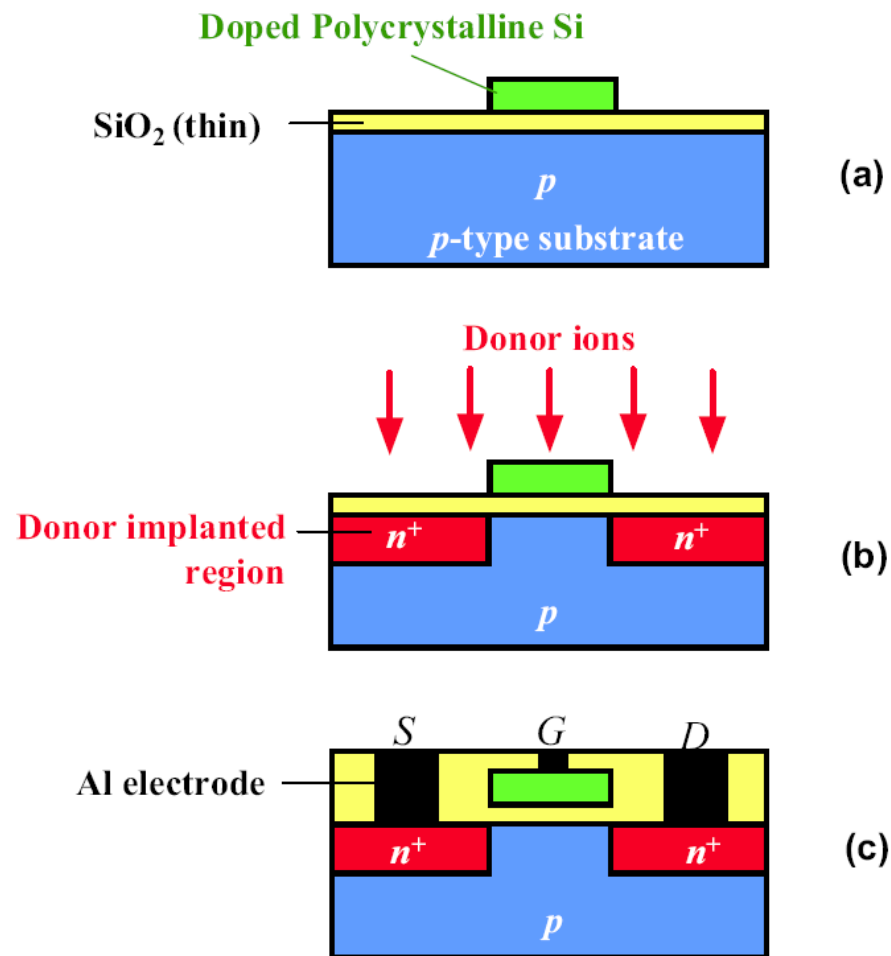
Schematic illustration of ion implantation for the control of  $V_{th}$ .

Fig 6.40



- (a) There is an overlap of the gate electrode with the source and drain regions and hence Additional capacitance between the gate and drain.
- (b)  $n^+$  type ion implantation extends the drain and source to line-up with the gate.

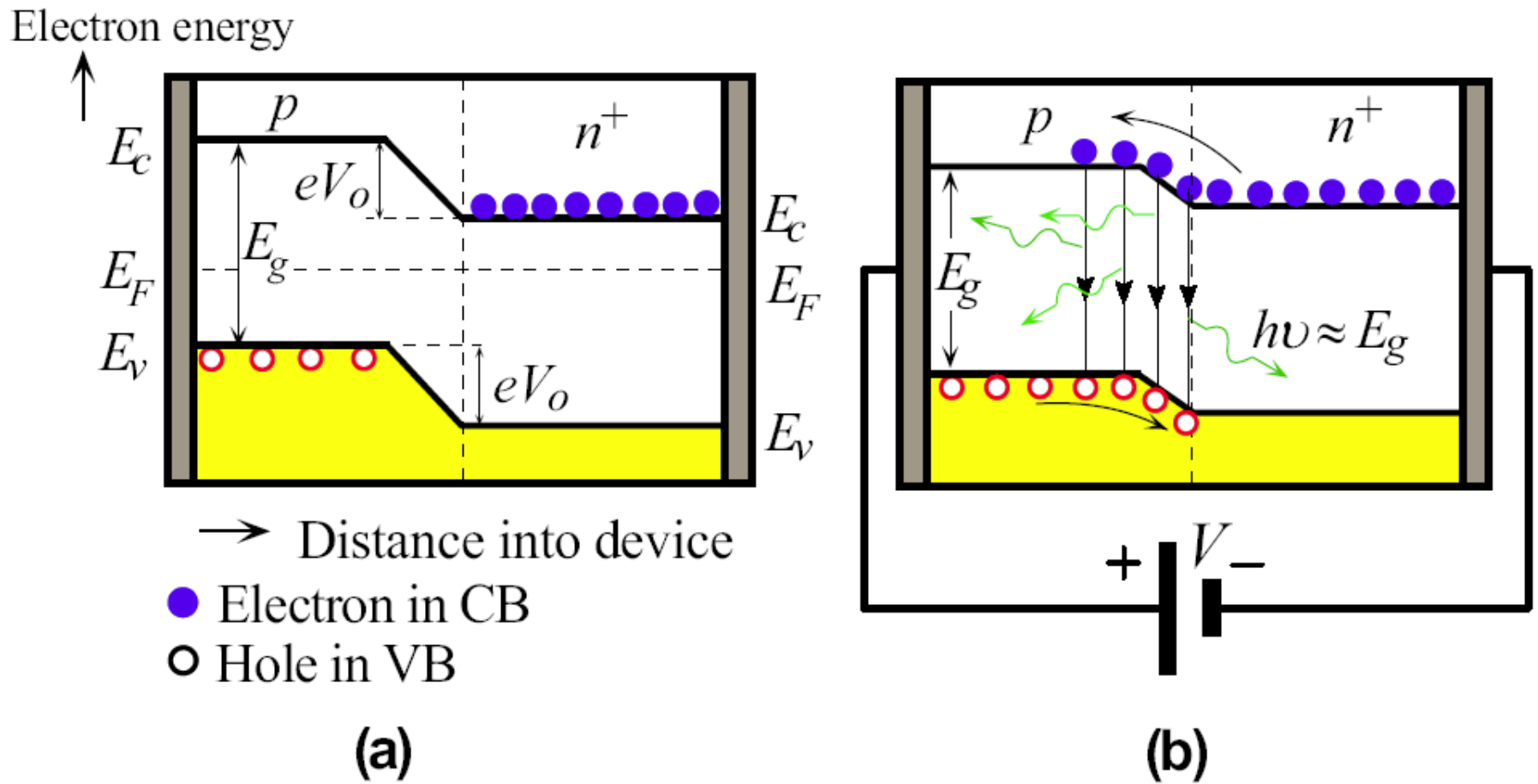
Fig 6.41



The poly-Si gate technology. (a) Poly-Si is deposited onto the oxide and the areas outside the gate dimensions are etched away. (b) The poly-Si gate acts as a mask during ion implantation of donors to form the  $n^+$  source and drain regions. (c) A simplified schematic sketch of the final poly-Si MOS transistor.

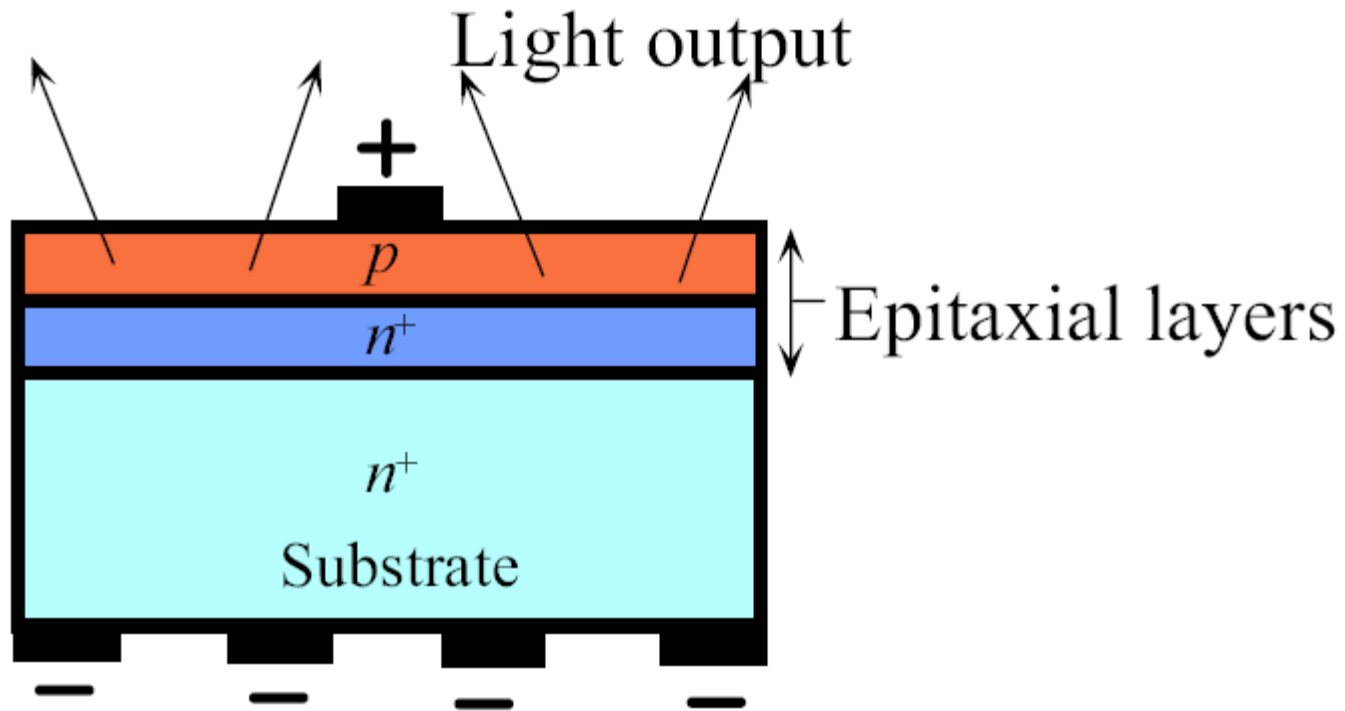
Fig 6.42





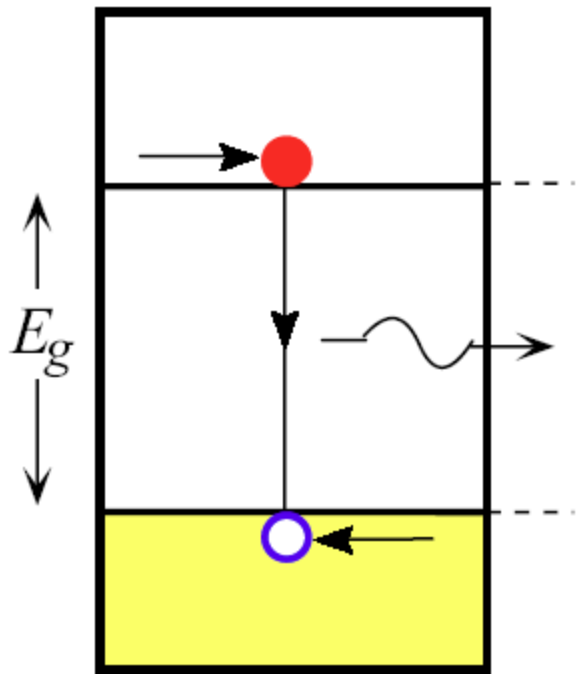
- (a) The energy band diagram of a  $p$ - $n^+$  (heavily  $n$ -type doped) junction without any bias. Built-in potential  $V_0$  prevents electrons from diffusing from  $n^+$  to  $p$  side.
- (b) The applied bias reduces  $V_0$  and thereby allows electrons to diffuse, be injected, into the  $p$ -side. Recombination around the junction and within the diffusion length of the electrons in the  $p$ -side leads to photon emission.

Fig 6.43

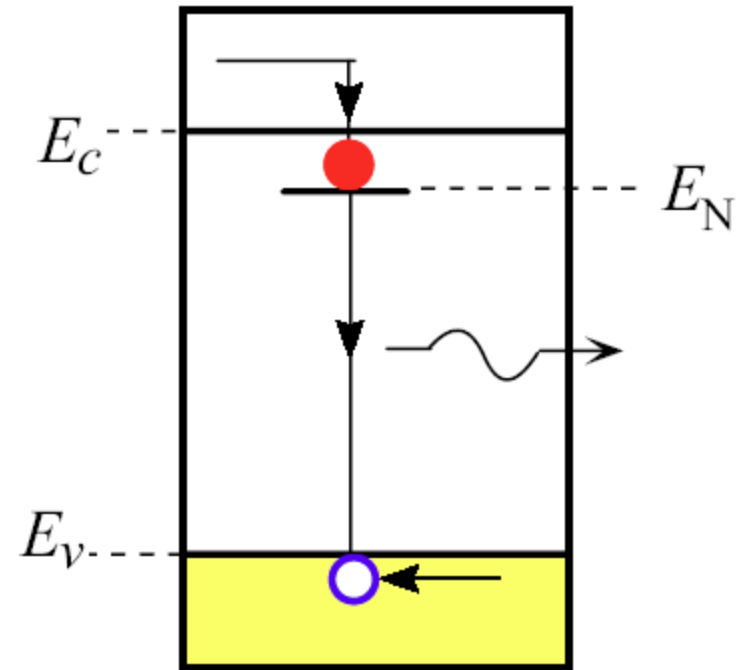


A schematic illustration of one possible LED device structure. First  $n^+$  is epitaxially grown on a substrate. A thin  $p$  layer is then epitaxially grown on the first layer.

Fig 6.44



(a)  $\text{GaAs}_{1-y}\text{P}_y$   $y < 0.45$



(b) N doped GaP

(a) Photon emission in a direct bandgap semiconductor.

(b) GaP is an indirect bandgap semiconductor. When doped with nitrogen there is an electron recombination center at  $E_N$ . Direct recombination between a captures electron at  $E_N$  and a hole emits a photon.

Fig 6.45

**Table 6.2** Selected LED semiconductor materials

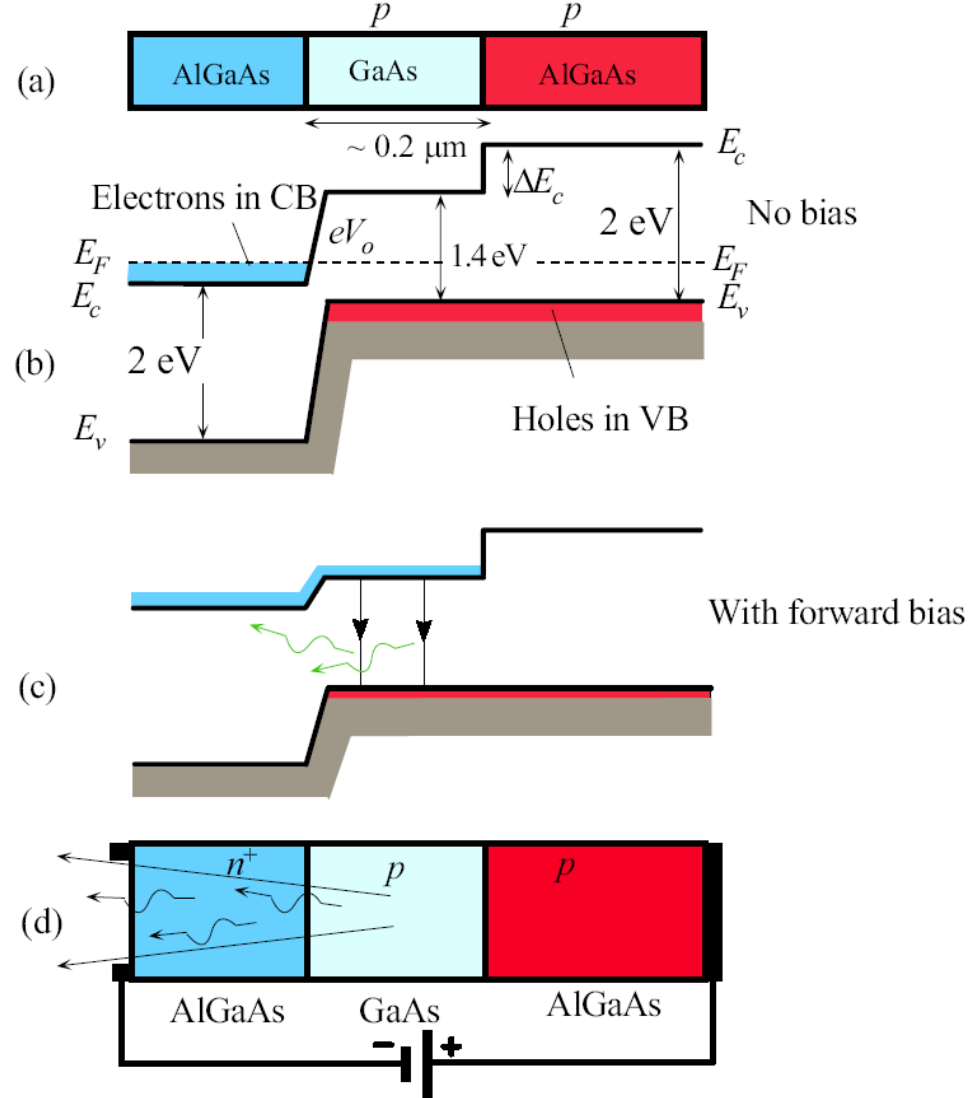
Semiconductor Active Layer	Structure	D or I	$\lambda$ (nm)	$\eta_{\text{external}}$ (%)	Comments
GaAs	DH	D	870–900	10	Infrared (IR)
$\text{Al}_x\text{Ga}_{1-x}\text{As}$ ( $0 < x < 0.4$ )	DH	D	640–870	3–20	Red to IR
$\text{In}_{1-x}\text{Ga}_x\text{As}_y\text{P}_{1-y}$ ( $y \approx 2.20x$ , $0 < x < 0.47$ )	DH	D	1–1.6 $\mu\text{m}$	>10	LEDs in communications
$\text{In}_{0.49}\text{Al}_x\text{Ga}_{0.51-x}\text{P}$	DH	D	590–630	>10	Amber, green, red; high luminous intensity
InGaN/GaN quantum well	QW	D	450–530	5–20	Blue to green
$\text{GaAs}_{1-y}\text{P}_y$ ( $y < 0.45$ )	HJ	D	630–870	< 1	Red to IR
$\text{GaAs}_{1-y}\text{P}_y$ ( $y > 0.45$ ) (N or Zn, O doping)	HJ	I	560–700	< 1	Red, orange, yellow
SiC	HJ	I	460–470	0.02	Blue, low efficiency
GaP (Zn)	HJ	I	700	2–3	Red
GaP (N)	HJ	I	565	< 1	Green

NOTE: Optical communication channels are at 850 nm (local network) and at 1.3 and 1.55  $\mu\text{m}$  (long distance). D = direct bandgap, I = indirect bandgap.  $\eta_{\text{external}}$  is typical and may vary substantially depending on the device structure. DH = double heterostructure, HJ = homojunction, QW = quantum well.

# Light Emitting Diodes (LED's)

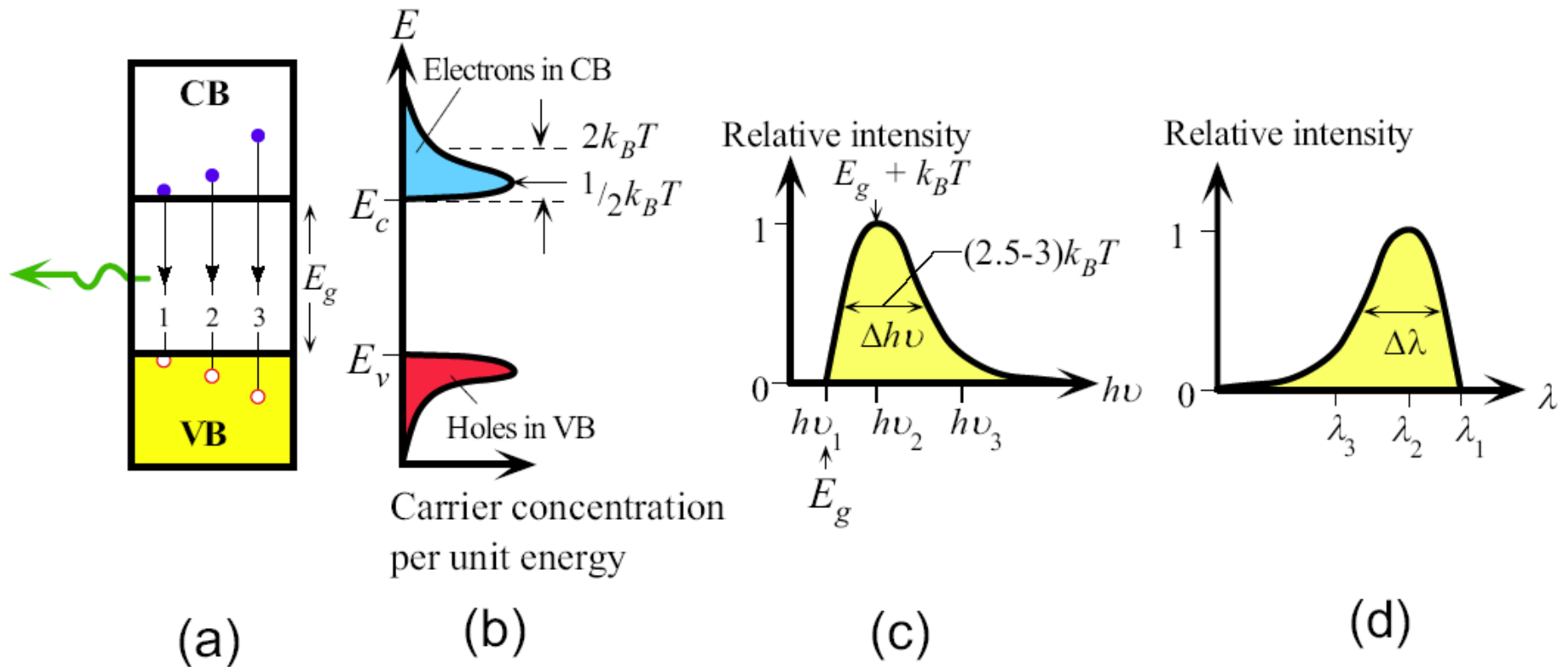
External efficiency,  $\eta_{\text{external}}$

$$\eta_{\text{external}} = \frac{P_{\text{out}} (\text{optical})}{IV} \times 100\%$$



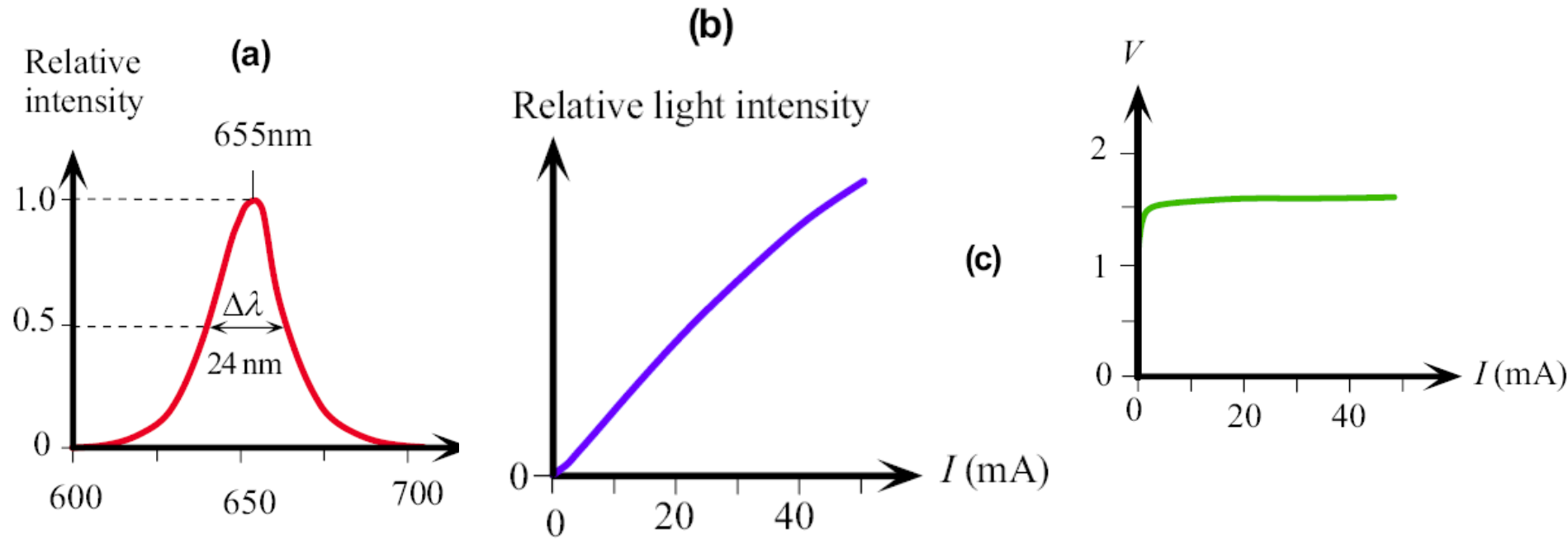
(a) A double heterostructure diode has two junctions which are between two different bandgap semiconductors (GaAs and AlGaAs). (b) A simplified energy band diagram with exaggerated features.  $E_F$  must be uniform. (c) Forward biased simplified energy band diagram. (d) Forward biased LED. Schematic illustration of photons escaping reabsorption in the AlGaAs layer and being emitted from the device.

Fig 6.46



(a) Energy band diagram with possible recombination paths. (b) Energy distribution of electrons in the CB and holes in the VB. The highest electron concentration is  $(1/2)k_B T$  above  $E_c$ . (c) The relative light intensity as a function of photon energy based on (b). (d) Relative intensity as a function of wavelength in the output spectrum based on (b) and (c).

Fig 6.47



(a) A typical output spectrum (relative intensity vs wavelength) from a red GaAsP LED. (b) Typical output light power vs. forward current. (c) Typical  $I$ - $V$  characteristics of a red LED. The turn-on voltage is around 1.5V

Fig 6.48



# LED Characteristics

Spread in the emitted photon energies,  $\Delta(h\nu)$ , is

$$\Delta(h\nu) \approx 3kT$$

LED spectral linewidth,  $\Delta\lambda$

$$\Delta\lambda = \lambda^2 \frac{3kT}{hc}$$

Example: At room temperature

$$\lambda = 1550\text{nm} \rightarrow \Delta\lambda = 150\text{nm}$$

# Solar Cells: Photovoltaics



NASA Dryden Flight Research Center Photo Collection

<http://www.dfrc.nasa.gov/gallery/photo/index.html>

NASA Photo: ED01-0209-5 Date: July 14, 2001 Photo by: Nick Galante/PMRF

The Helios Prototype flying wing is shown near the Hawaiian islands of Niihau and Lehua during its first test flight on solar power from the U.S. Navy's Pacific Missile Range Facility.

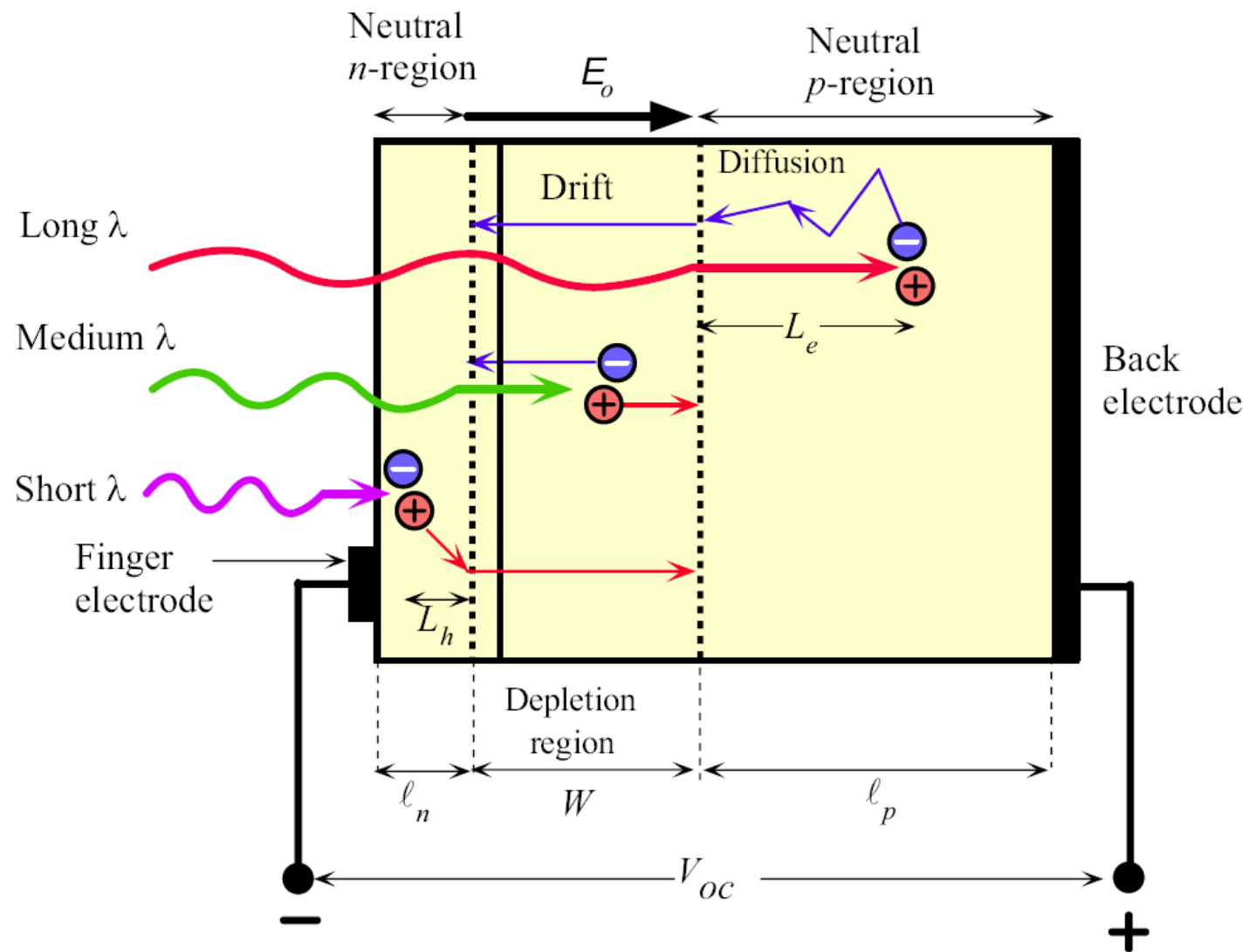
**|SOURCE: Courtesy of NASA, Dryden Flight Center**

From *Principles of Electronic Materials and Devices, Third Edition*, S.O. Kasap (© McGraw-Hill, 2005)



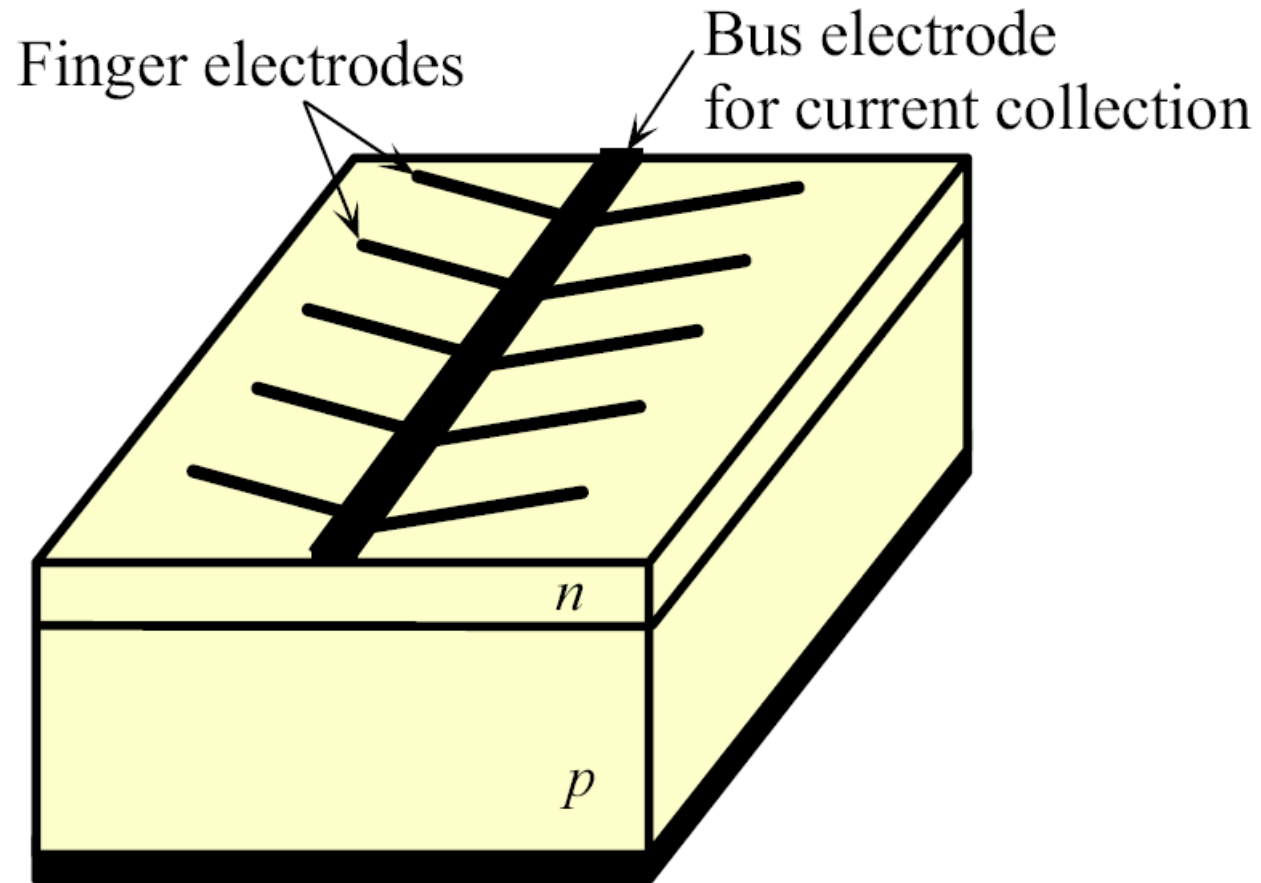
**Solar cell inventors at Bell Labs (left to right) Gerald Pearson, Daryl Chapin and Calvin Fuller are checking a Si solar cell sample for the amount of voltage produced (1954).**

**|SOURCE: Courtesy of Bell Labs, Lucent Technologies**



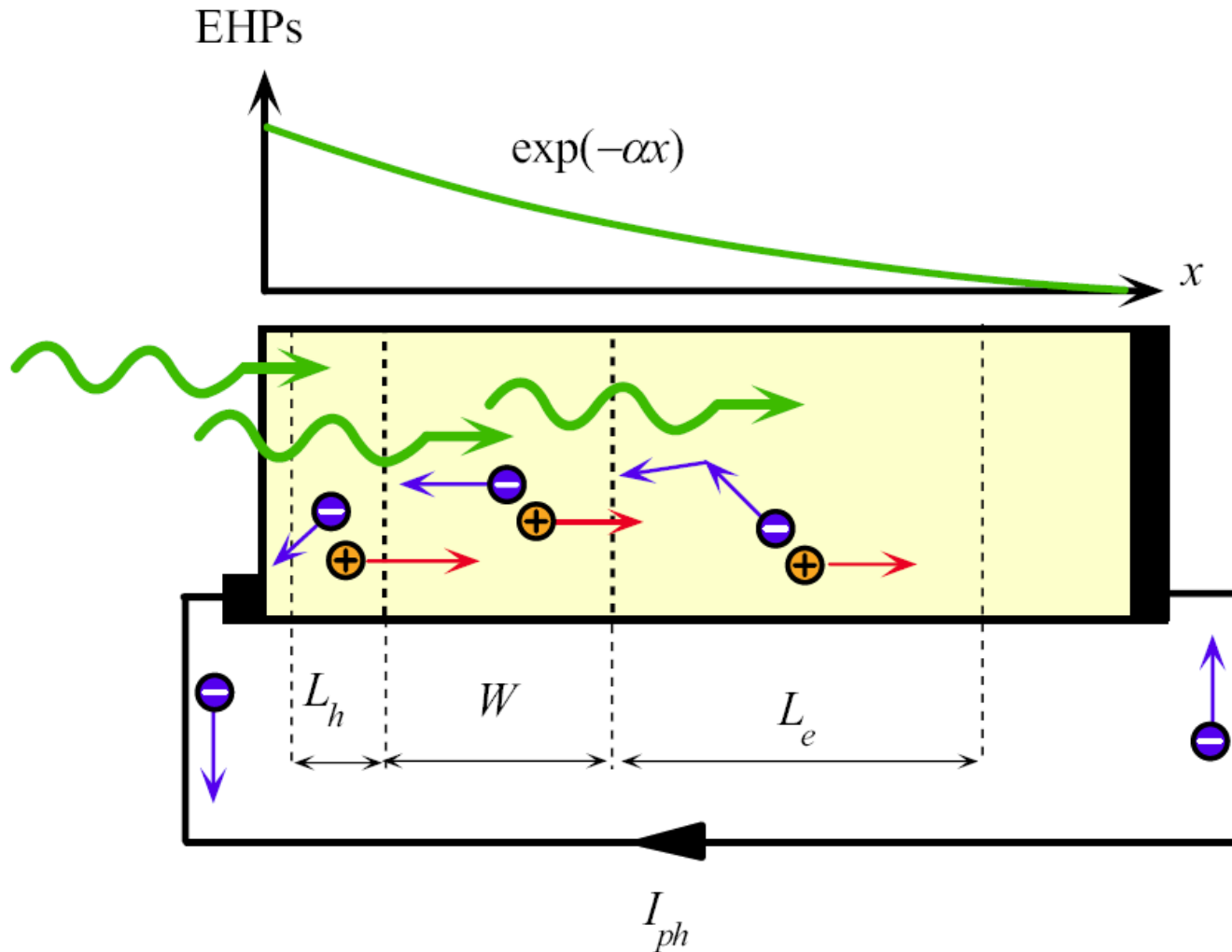
The principle of operation of the solar cell (exaggerated features to highlight principles)

Fig 6.49



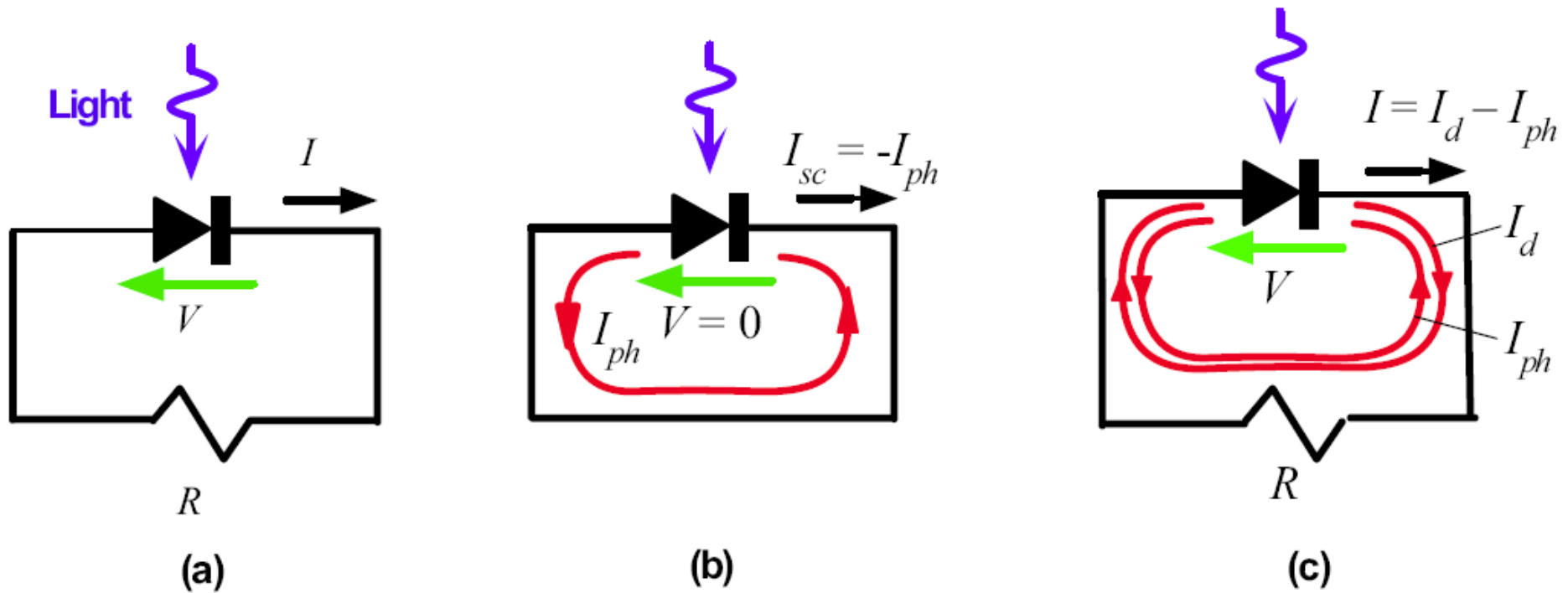
Finger electrodes on the surface of a solar cell reduce the series resistance.

Fig 6.50



Photogenerated carriers within the volume  $L_h + W + L_e$  give rise to a photocurrent  $I_{ph}$ . The variation in the photogenerated EHP concentration with distance is also shown where  $\alpha$  is the absorption coefficient at the wavelength of interest.

Fig 6.51



- (a) The solar cell connected to an external load  $R$  and the convention for the definitions of positive voltage and positive current.
- (b) The solar cell in short circuit. The current is the photocurrent,  $I_{ph}$ .
- (c) The solar cell driving an external load  $R$ . There is a voltage  $V$  and current  $I$  in the circuit.

Fig 6.52

# Solar Cells

## Short circuit solar cell current in light

$$I_{\text{sc}} = -I_{\text{ph}} = -KI$$

↑  
Photocurrent generated by light

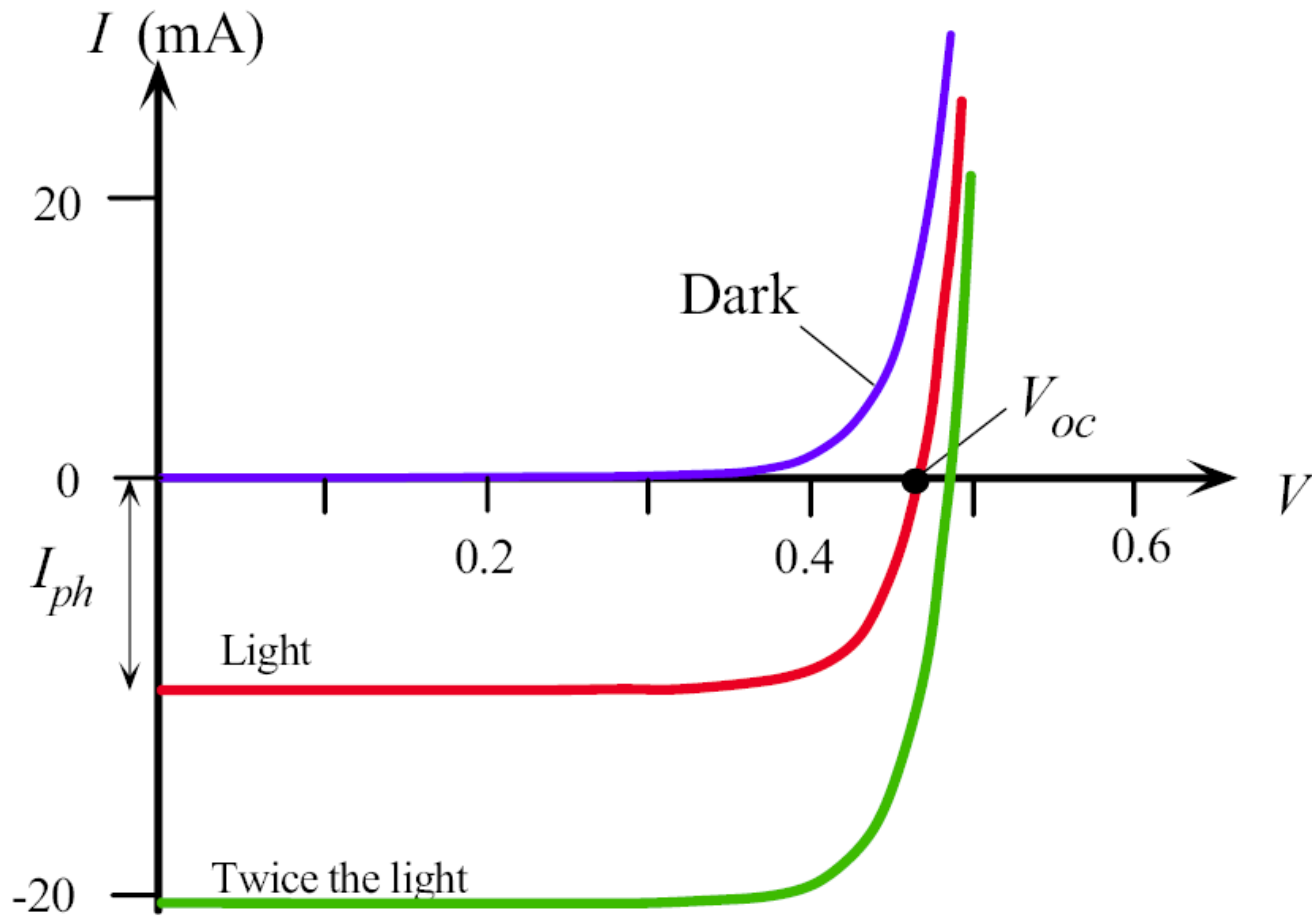
↖ ↗  
Constant that depends on the particular device      Light intensity

## Solar cell $I$ - $V$

$$I = -I_{\text{ph}} + I_o \left[ \exp\left(\frac{eV}{\eta kT}\right) - 1 \right]$$

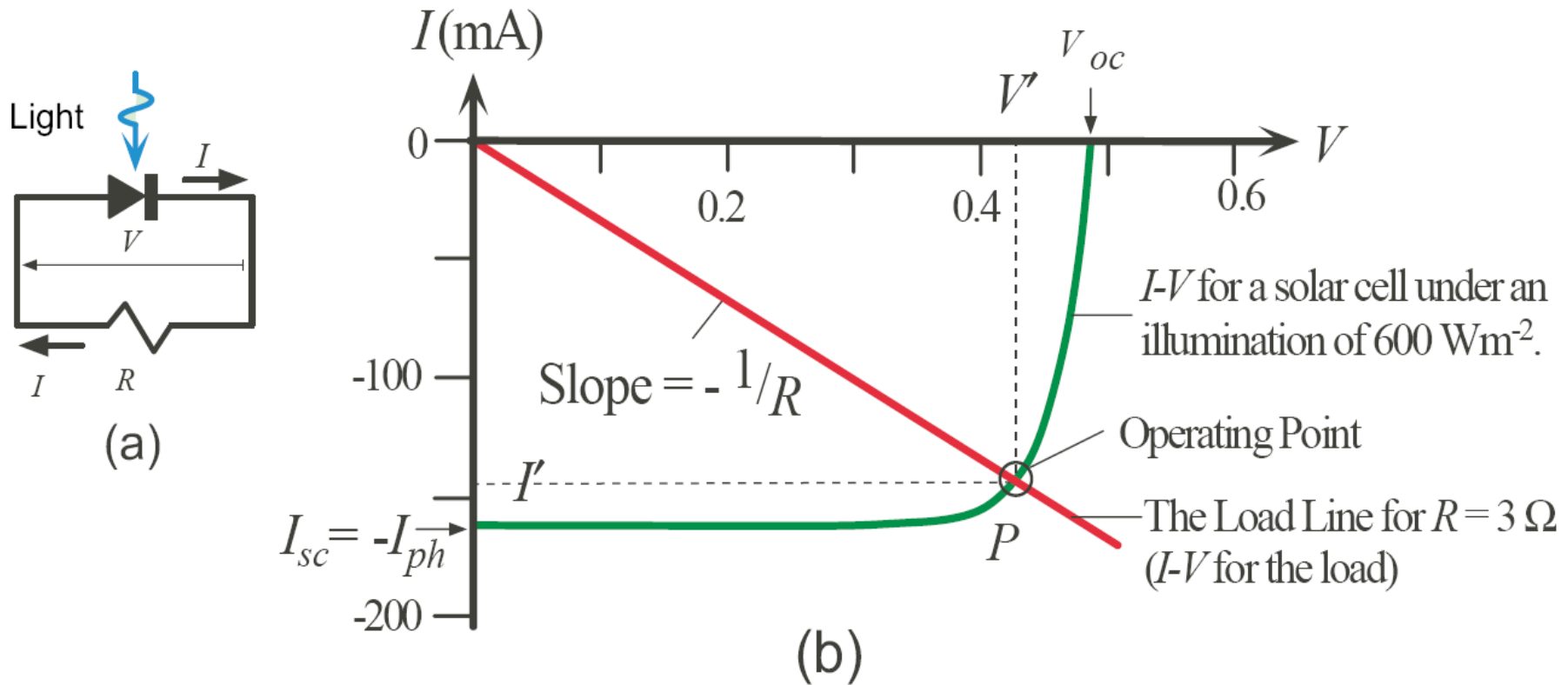
where  $I_o$  is the reverse saturation current and  $\eta$  is the ideality factor: 1 - 2





Typical  $I$ - $V$  characteristics of a Si solar cell. The short circuit current is  $I_{ph}$  and the open circuit voltage is  $V_{OC}$ . The  $I$ - $V$  curves for positive current requires an external bias voltage. Photovoltaic operation is always in the negative current region.

Fig 6.53



(a) When a solar cell drives a load  $R$ .  $R$  has the same voltage as the solar cell but the current through it is in the opposite direction to the convention that current flows from high to low potential. (b) The current  $I'$  and voltage  $V'$  in the circuit of (a) can be found from a load line construction. Point  $P$  is the operating point ( $I'$ ,  $V'$ ). The load line is for  $R = 3 \Omega$ .

Fig 6.54

# Solar Cells

## The load line

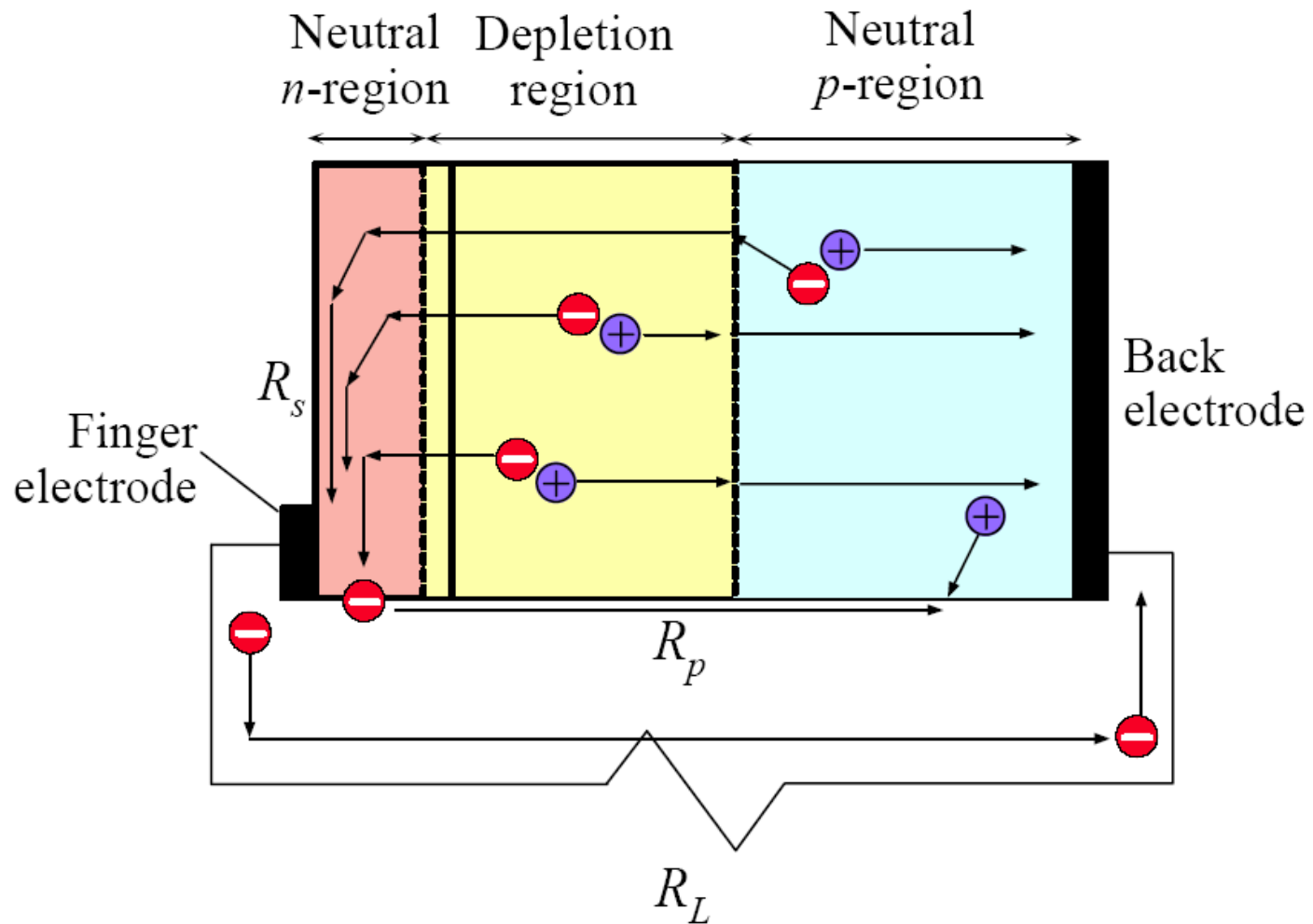
$$I = -\frac{V}{R}$$

The actual current  $I'$  and voltage  $V'$  in the circuit must satisfy both the  $I$  -  $V$  characteristics of the solar cell and the load.

## Definition of fill factor

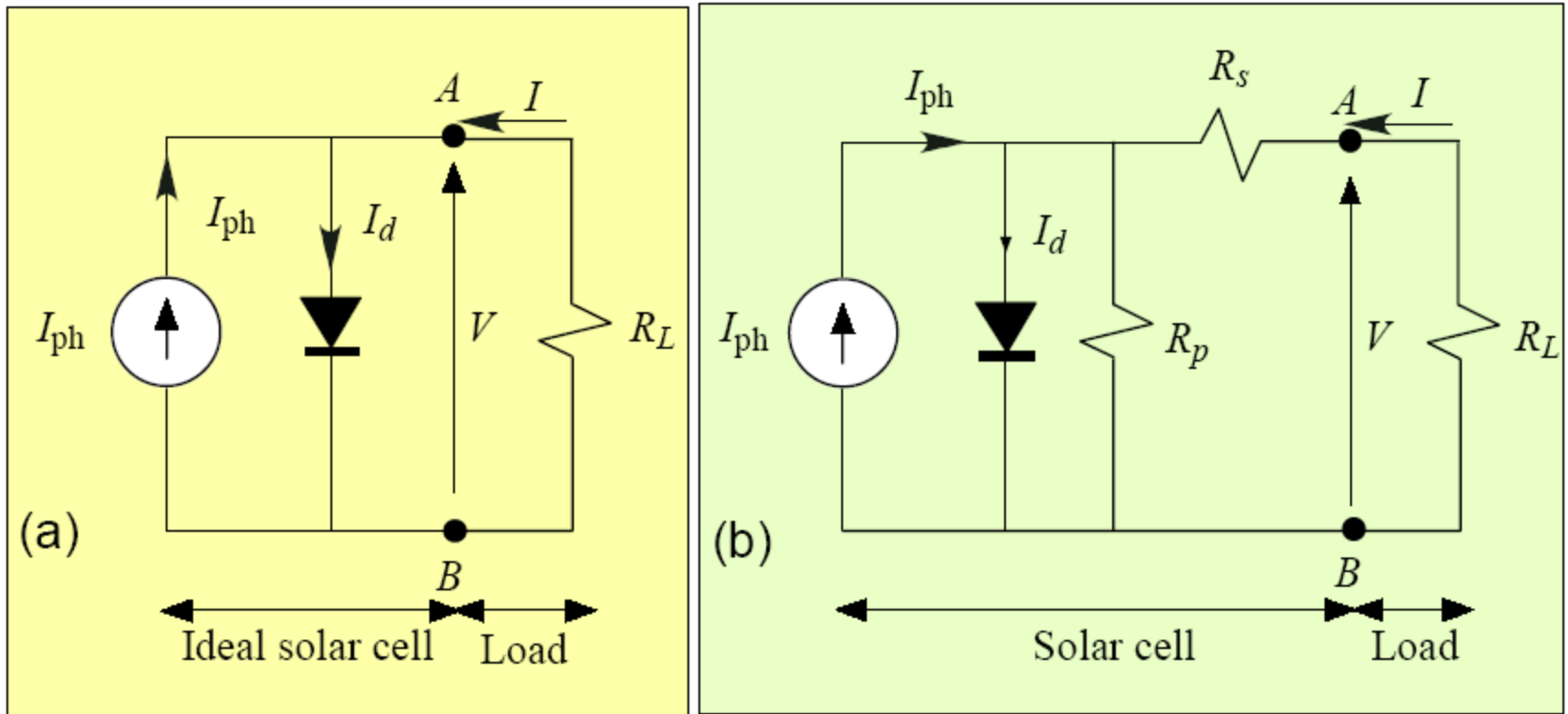
$$\text{FF} = \frac{I_m V_m}{I_{\text{sc}} V_{\text{oc}}}$$

The FF is a measure of the closeness of the solar cell  $I$ - $V$  curve to the rectangular shape (the ideal shape).



Series and shunt resistances and various fates of photogenerated EHPs.

Fig 6.55

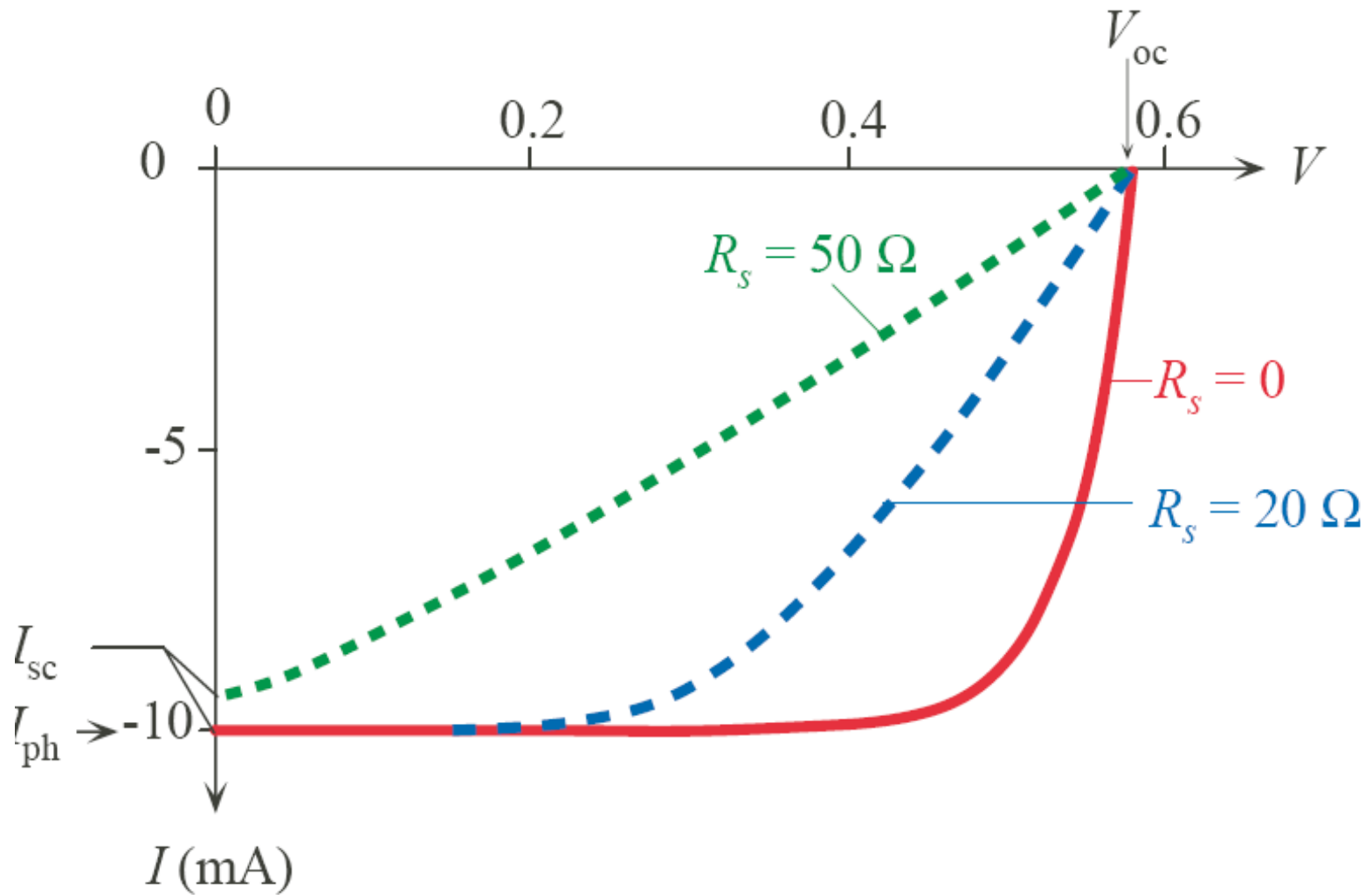


The equivalent circuit of a solar cell

(a) Ideal pn junction solar cell

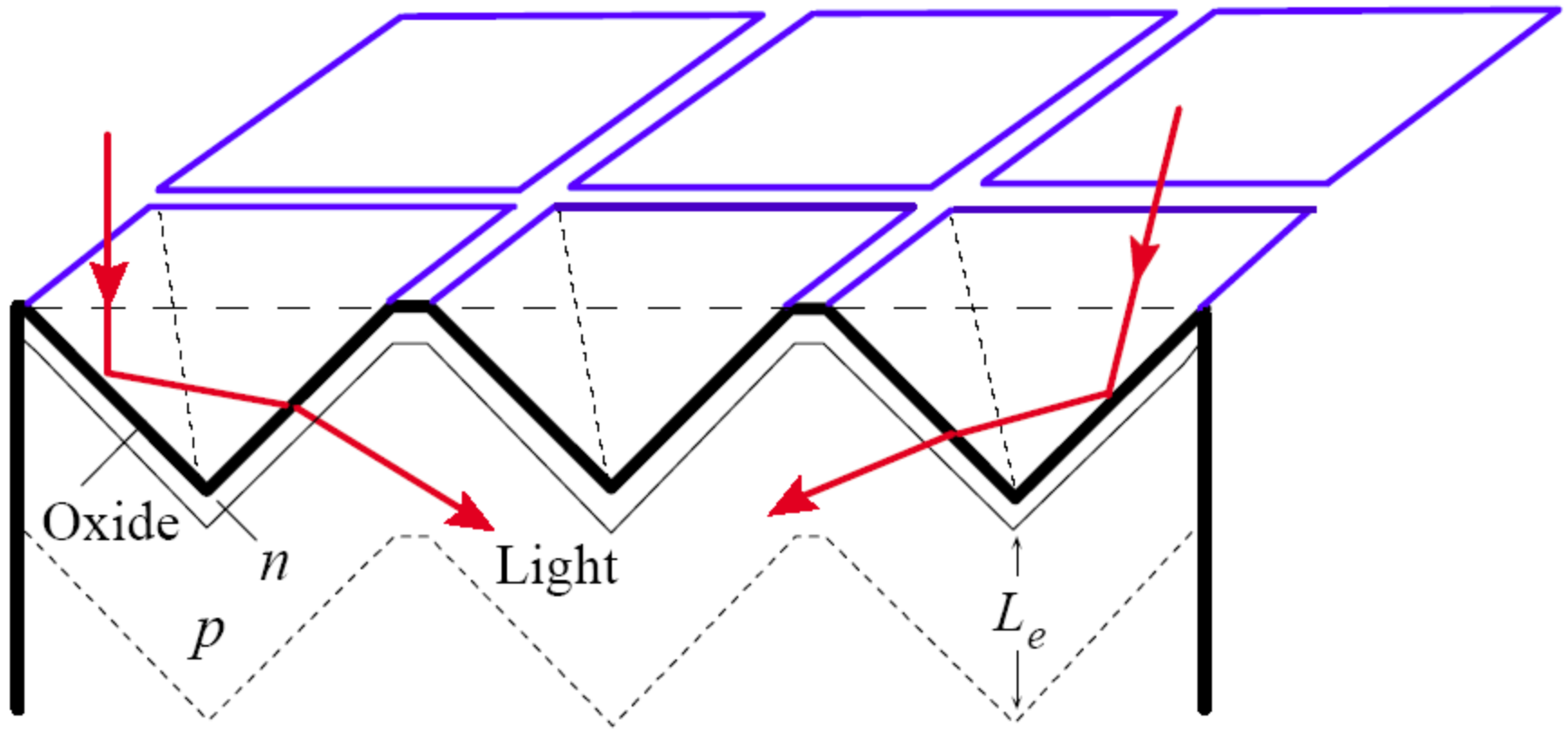
(b) Parallel and series resistances  $R_s$  and  $R_p$ .

Fig 6.56



The series resistance broadens the  $I$ - $V$  curve and reduces the maximum available power and hence the overall efficiency of the solar cell. The example is a Si solar cell with  $\eta \approx 1.5$  and  $I_o \approx 3 \times 10^{-6}$  mA. Illumination is such that the photocurrent  $I_{ph} = 10$  mA.

Fig 6.57



Inverted pyramid textured surface substantially reduces reflection losses and increases absorption probability in the device.

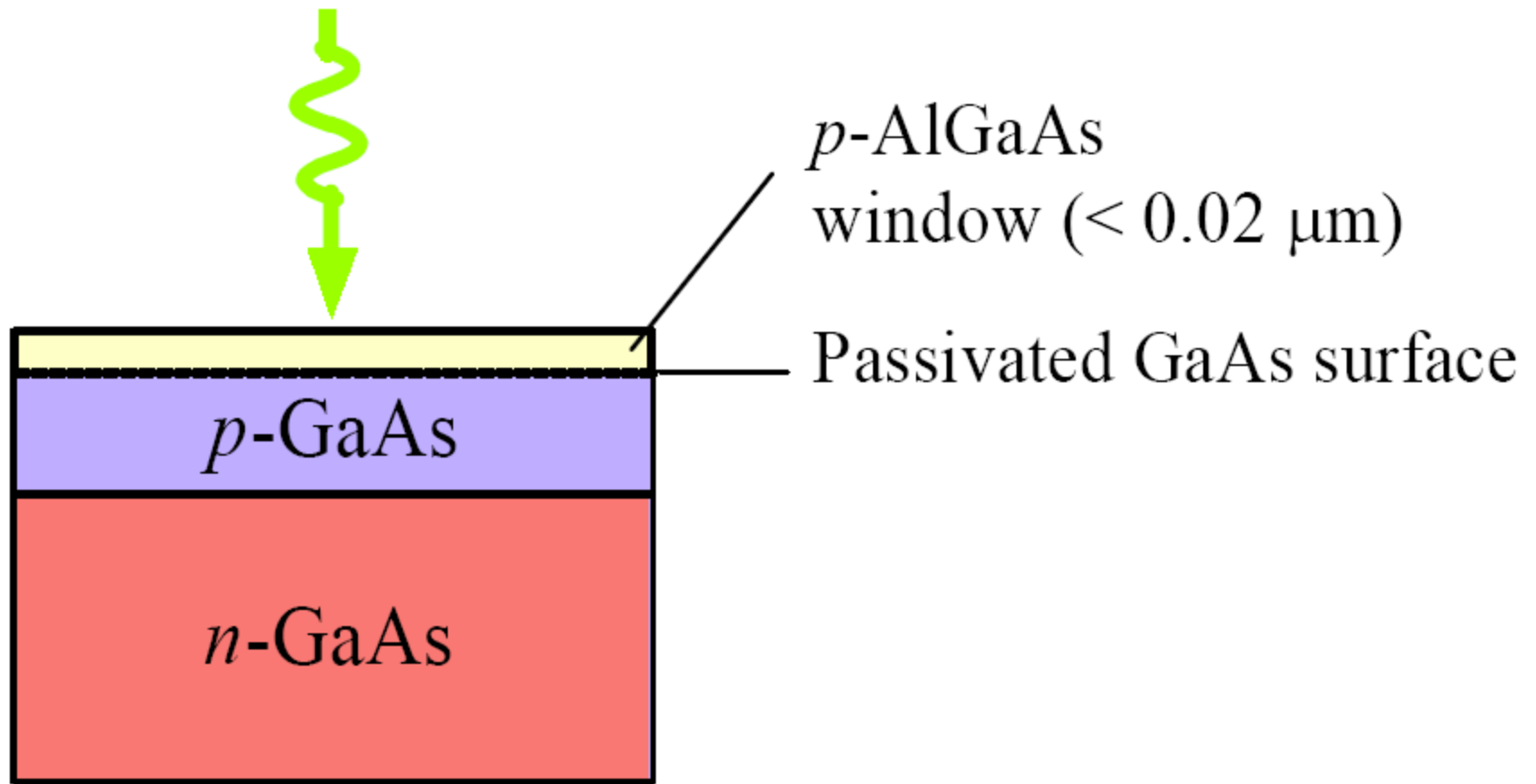
Fig 6.58

**Table 6.3** Typical characteristics of various solar cells at room temperature under AM1.5 illumination of  $1000 \text{ W m}^{-2}$ 

Semiconductor	$E_g$ (eV)	$V_{oc}$ (V)	$J_{sc}$ (mA cm $^{-2}$ )	FF	$\eta$ (%)	Comments
Si, single crystal	1.1	0.5–0.7	42	0.7–0.8	16–24	Single crystal, PERL
Si, polycrystalline	1.1	0.5–0.65	38	0.7–0.8	12–19	
Amorphous Si:Ge:H film					8–13	
						Amorphous film with tandem structure, convenient large-area fabrication
GaAs, single crystal	1.42	1.02	28	0.85	24–25	Different bandgap materials in tandem increases absorption efficiency
GaAlAs/GaAs, tandem		1.03	27.9	0.864	24.8	
GaInP/GaAs, tandem		2.5	14	0.86	25–30	Different bandgap materials in tandem increases absorption efficiency
CdTe, thin film	1.5	0.84	26	0.75	15–16	
InP, single crystal	1.34	0.87	29	0.85	21–22	
CuInSe $_2$	1.0				12–13	

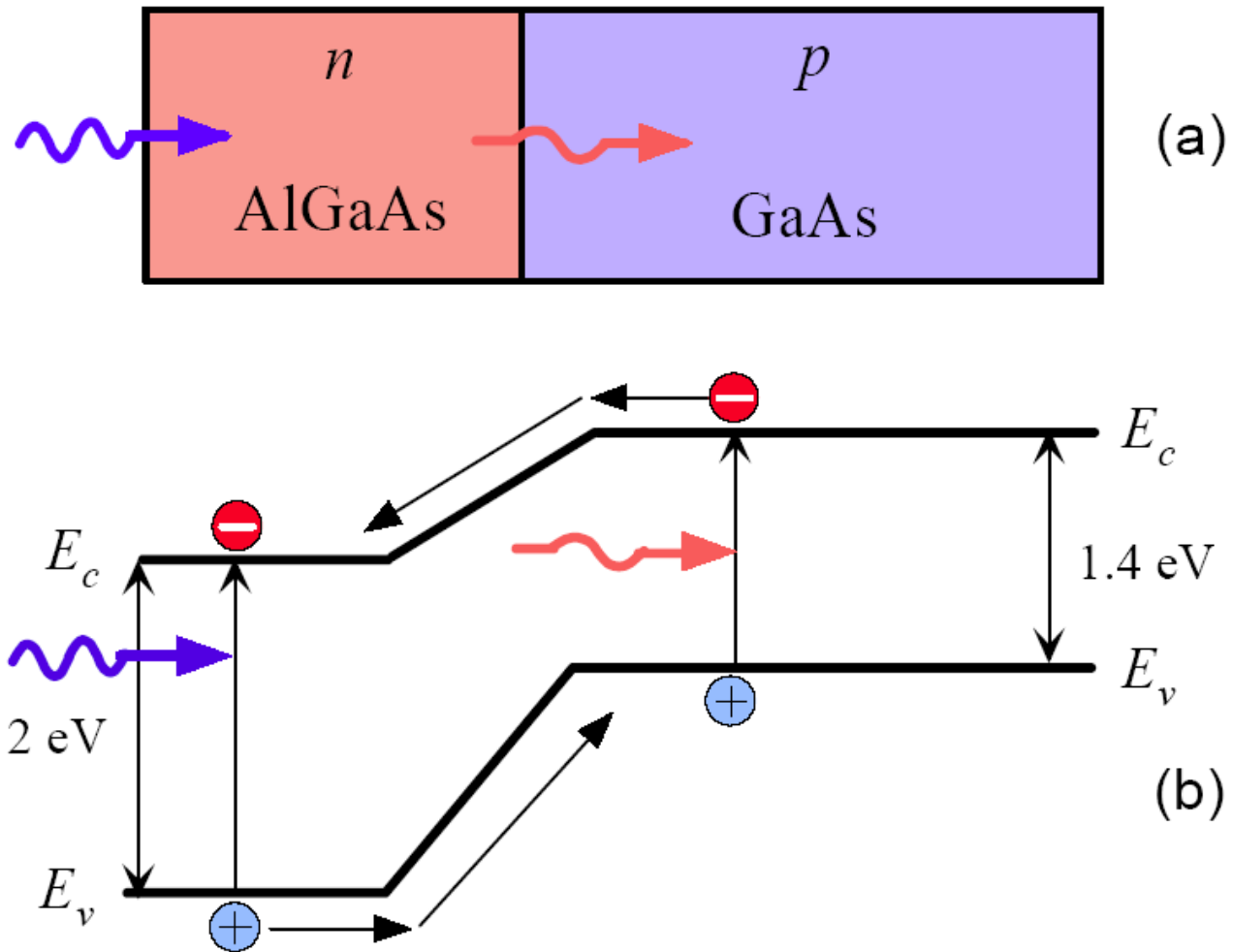
NOTE: AM1.5 refers to a solar illumination of "Air Mass 1.5," which represents solar radiation falling on the Earth's surface with a total intensity (or irradiance) of  $1000 \text{ W m}^{-2}$ . AM1.5 is widely used for comparing solar cells.





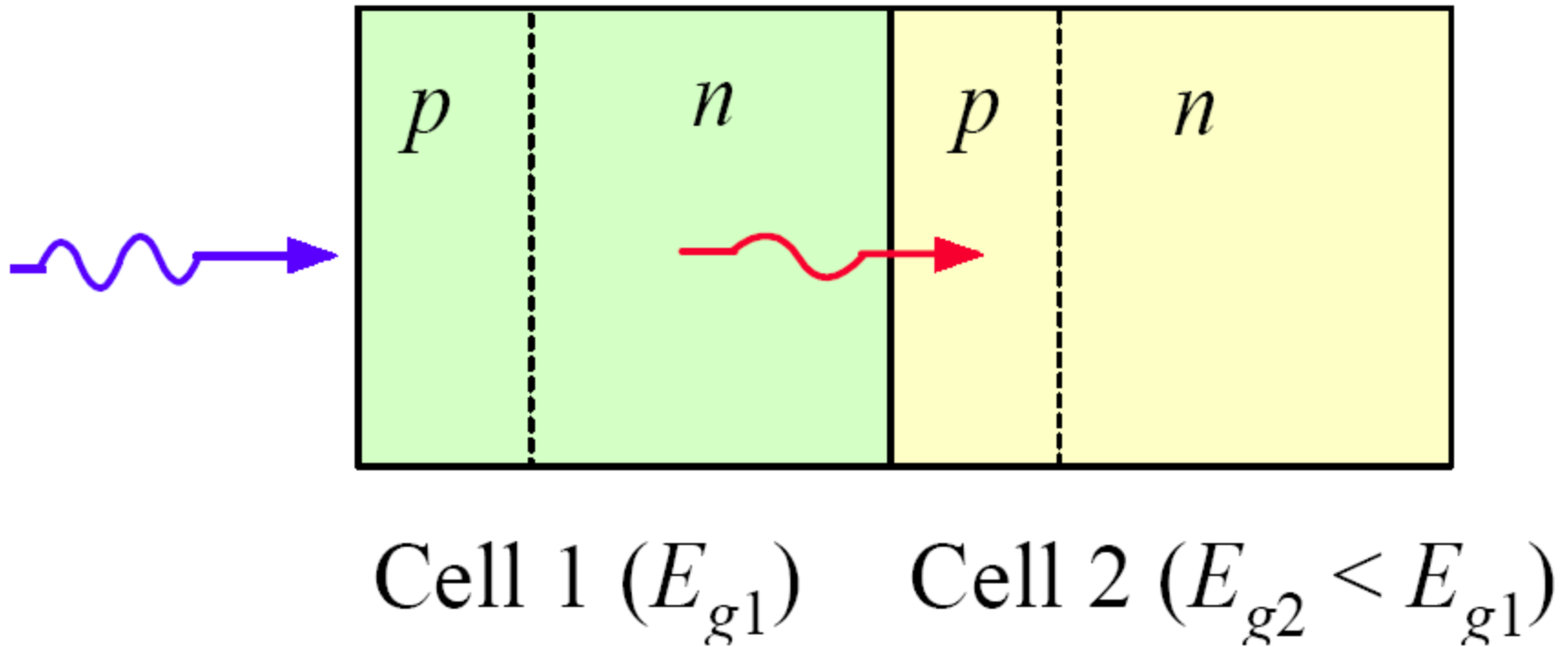
AlGaAs window layer on GaAs passivates the surface states and thereby increases the photogeneration efficiency.

Fig 6.59



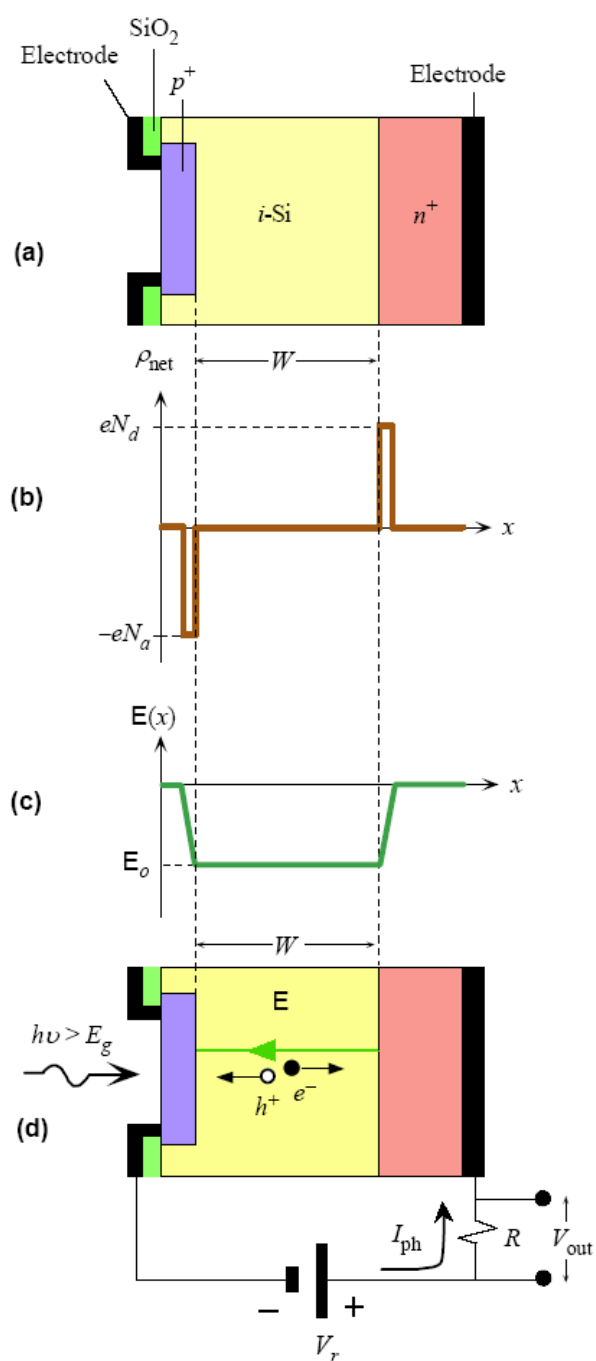
A heterojunction solar cell between two different bandgap semiconductors (GaAs and AlGaAs)

Fig 6.60



A tandem cell. Cell 1 has a wider bandgap and absorbs energetic photons with  $h\nu > E_{g1}$ . Cell 2 absorbs photons that pass cell 1 and have  $h\nu > E_{g2}$ .

Fig 6.61



- (a) The schematic structure of an idealized pin Photodiode
- (b) The net space charge density across the photodiode.
- (c) The built-in field across the diode.
- (d) The pin photodiode in photodetection is reverse biased.

Fig 6.62

# *pin* Diodes, photodiodes and solar cells

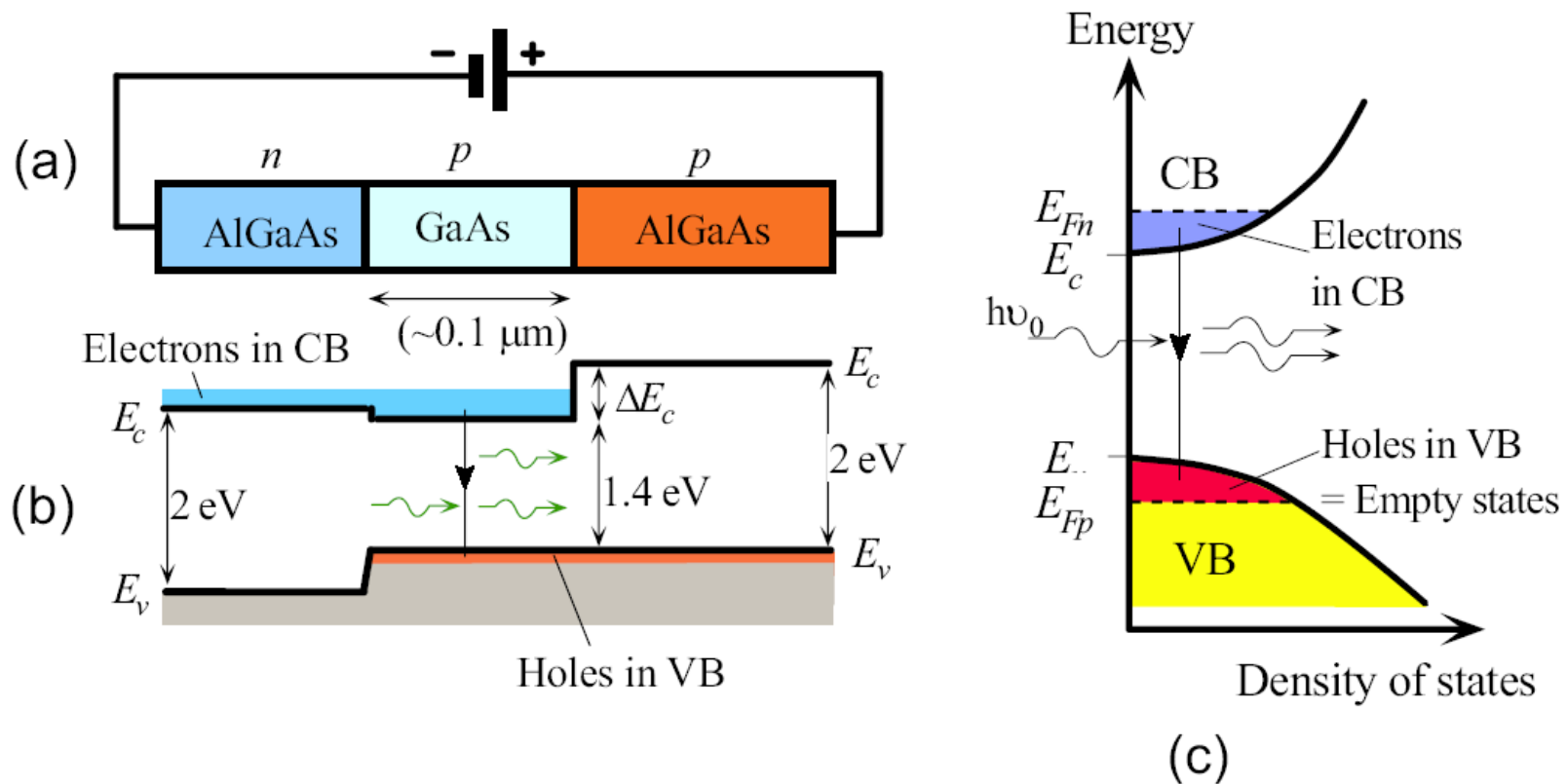
## Junction capacitance of *pin*

$$C_{\text{dep}} = \frac{\epsilon_o \epsilon_r A}{W}$$

where  $A$  is the cross-sectional area and  $\epsilon_o \epsilon_r$  is the permittivity of the semiconductor (Si) and  $W$  is the width of the *i*-region.

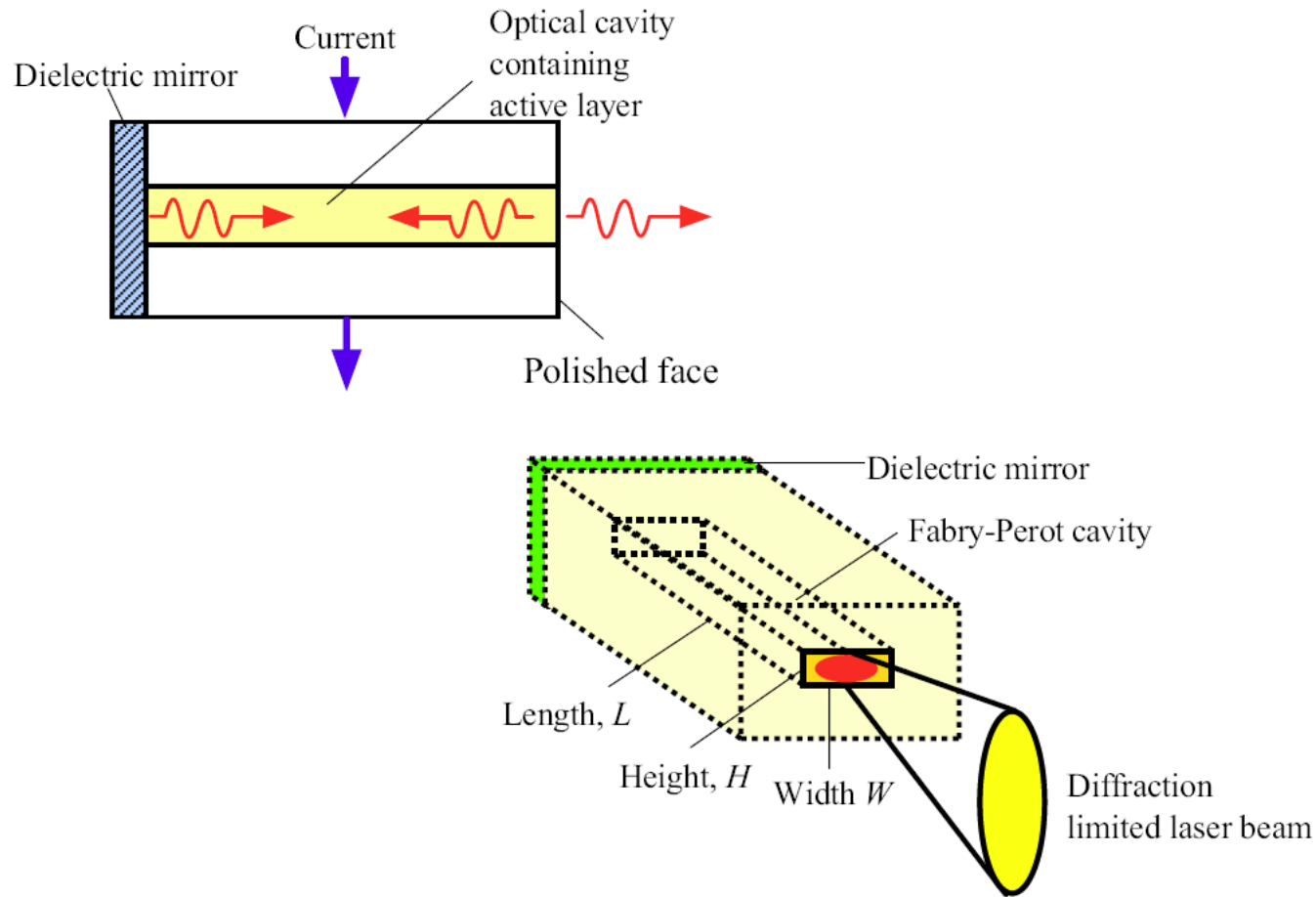
## Reverse biased *pin*: the electric field $E$ in the *i*-region

$$E = E_o + \frac{V_r}{W} \approx \frac{V_r}{W} \quad \text{if } V_r \gg V_o$$



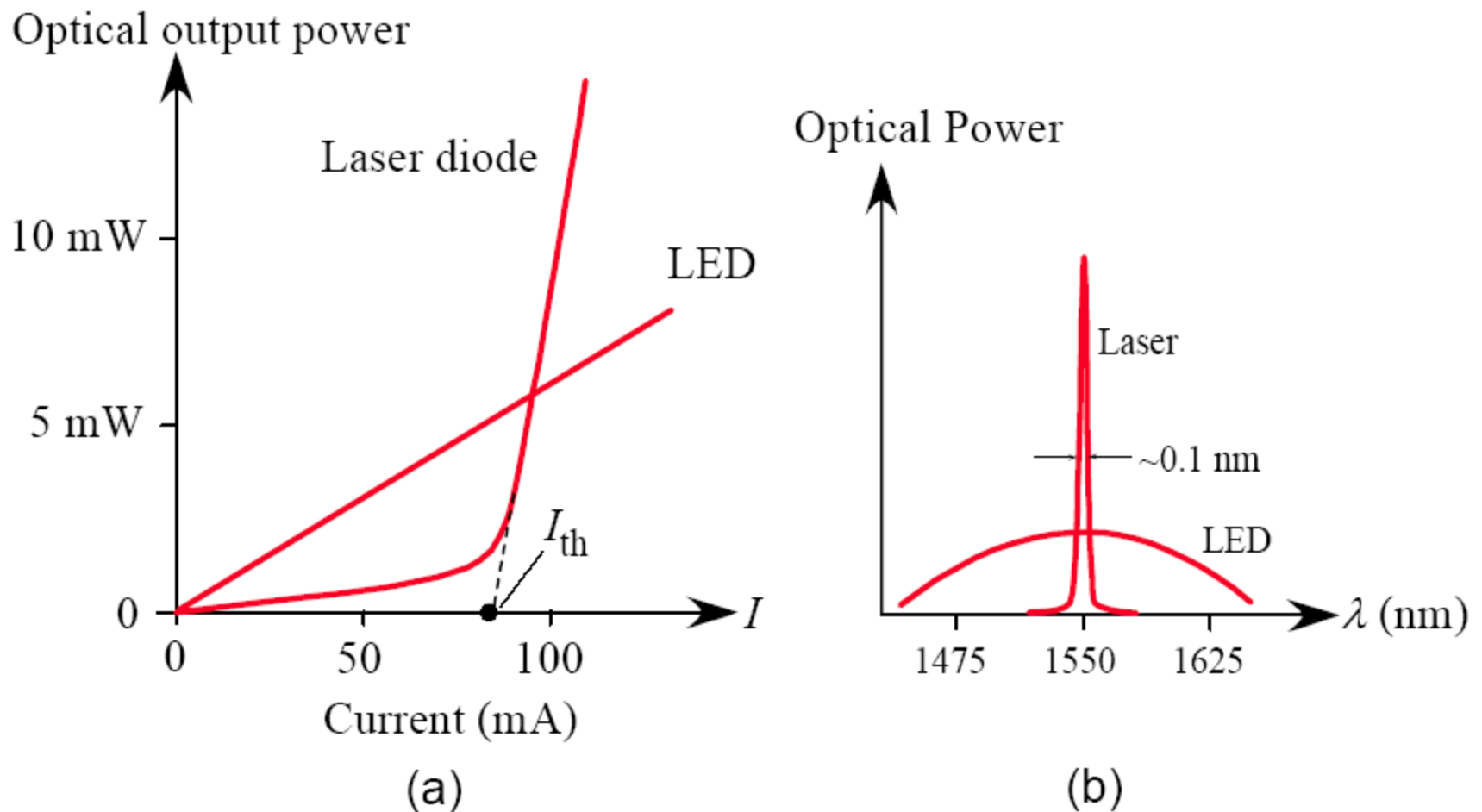
- (a) A double heterostructure diode has two junctions which are between two different bandgap semiconductors (GaAs and AlGaAs).
- (b) Simplified energy band diagram under a large forward bias. Lasing recombination takes place in the  $p$ -GaAs layer, the active layer.
- (c) The density of states and energy distribution of electrons and holes in the conduction and valence bands in the active layer.

Fig 6.63



Semiconductor lasers have an optical cavity to build up the required electromagnetic oscillations. In this example, one end of the cavity has a Bragg distributed reflector, a reflection grating, that reflects only certain wavelengths back into the cavity.

Fig 6.64



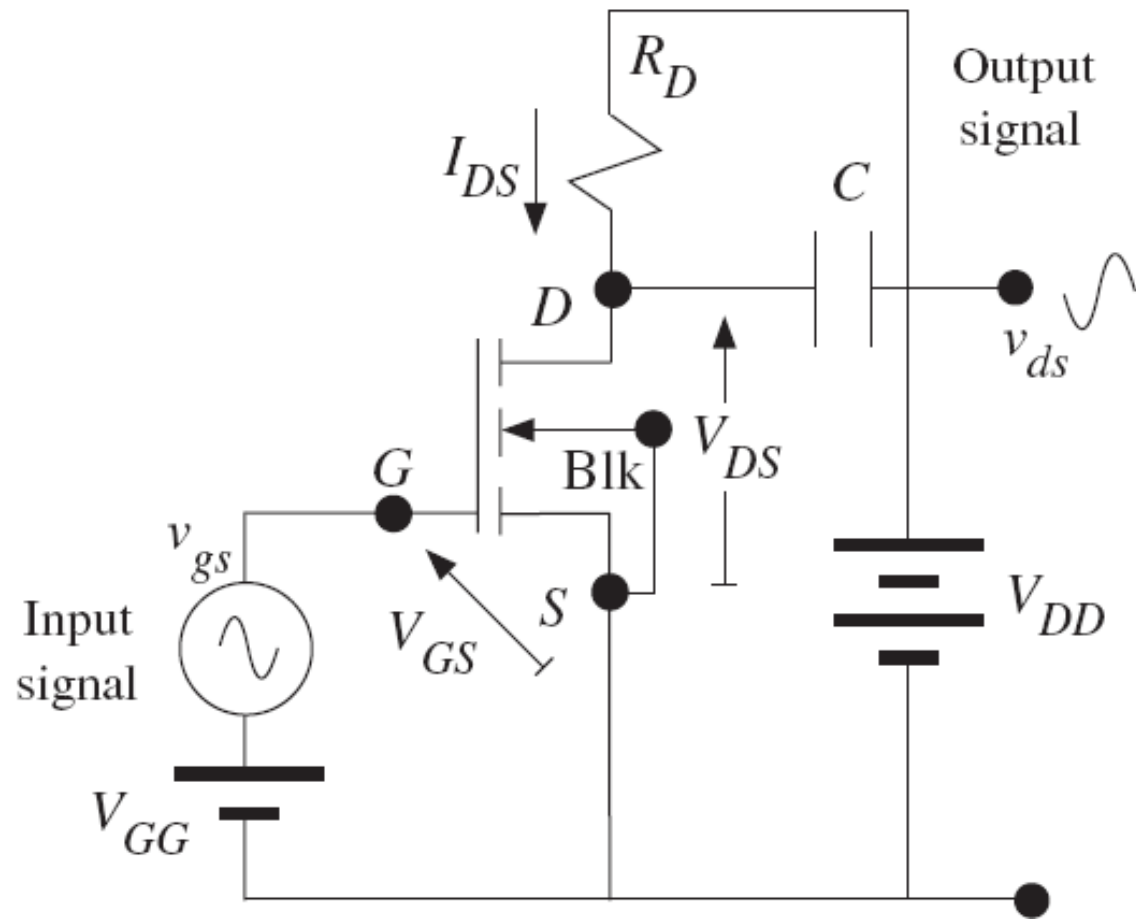
- (a) Typical optical power output vs. forward current for a laser diode and an LED.  
(b) Comparison of spectral output characteristics.

Fig 6.65



**Table 6.4** Capacitance at various values of reverse bias ( $V_r$ )

$V_r$ (V)	1	2	3	5	10	15	20
$C$ (pF)	38.3	30.7	26.4	21.3	15.6	12.9	11.3

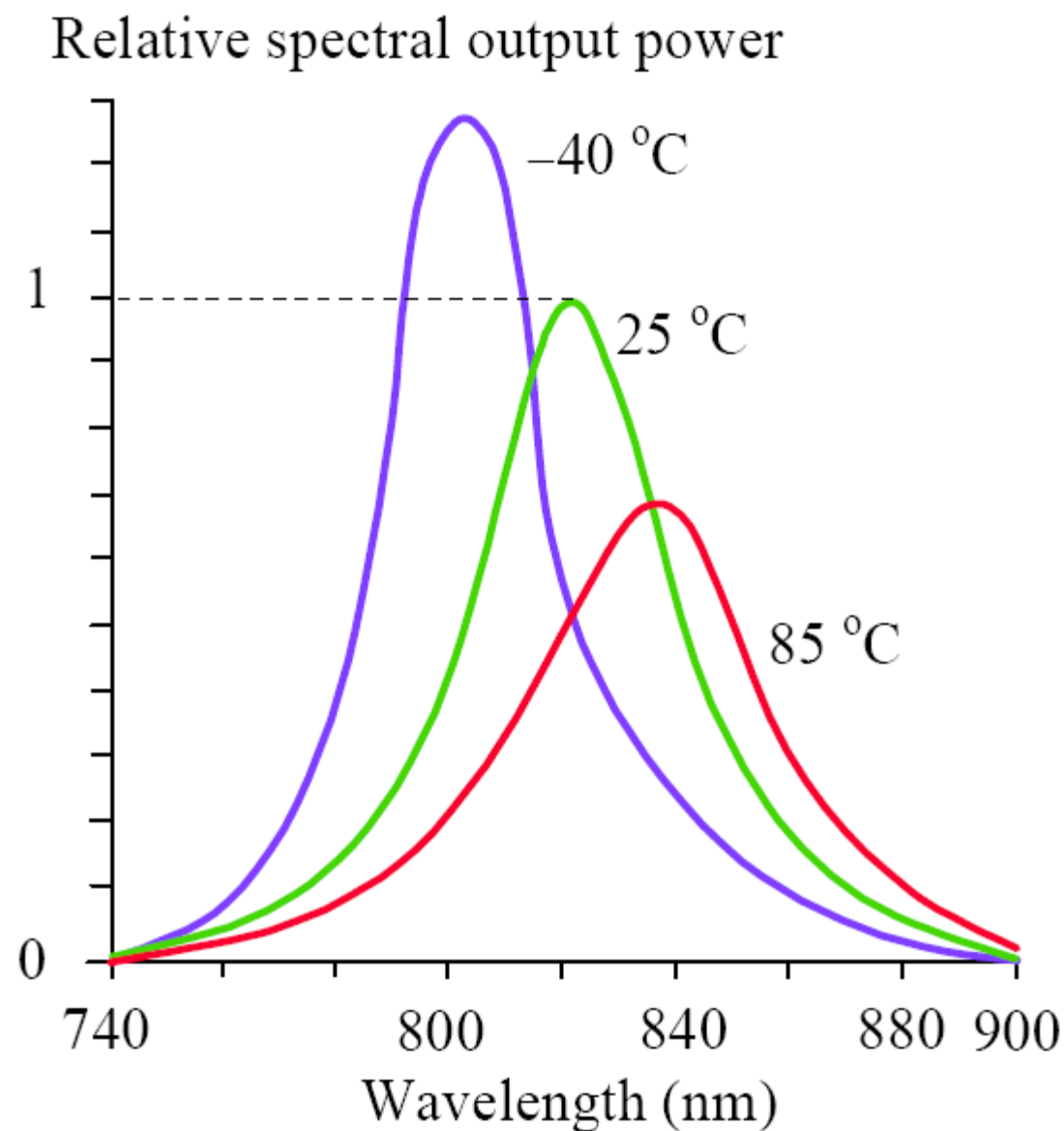


NMOSFET amplifier.

Fig 6.67

**Table 6.6** Linewidth  $\Delta\lambda_{1/2}$  between half-points in the output spectrum (intensity versus wavelength) of GaAs and AlGaAs LEDs

	Peak wavelength of emission $\lambda$ (nm)							
	650	810	820	890	950	1150	1270	1500
$\Delta\lambda_{1/2}$ (nm)	22	36	40	50	55	90	110	150
Material (direct $E_g$ )	AlGaAs	AlGaAs	AlGaAs	GaAs	GaAs	InGaAsP	InGaAsP	InGaAsP



The output spectrum from AlGaAs LED. Values normalized to peak emission at 25 °C