

August 1986 Revised March 2000

DM74LS138 • DM74LS139 Decoder/Demultiplexer

General Description

These Schottky-clamped circuits are designed to be used in high-performance memory-decoding or data-routing applications, requiring very short propagation delay times. In high-performance memory systems these decoders can be used to minimize the effects of system decoding. When used with high-speed memories, the delay times of these decoders are usually less than the typical access time of the memory. This means that the effective system delay introduced by the decoder is negligible.

The DM74LS138 decodes one-of-eight lines, based upon the conditions at the three binary select inputs and the three enable inputs. Two active-low and one active-high enable inputs reduce the need for external gates or inverters when expanding. A 24-line decoder can be implemented with no external inverters, and a 32-line decoder requires only one inverter. An enable input can be used as a data input for demultiplexing applications.

The DM74LS139 comprises two separate two-line-to-four-line decoders in a single package. The active-low enable input can be used as a data line in demultiplexing applications

All of these decoders/demultiplexers feature fully buffered inputs, presenting only one normalized load to its driving circuit. All inputs are clamped with high-performance Schottky diodes to suppress line-ringing and simplify system design.

Features

- Designed specifically for high speed: Memory decoders
 - Data transmission systems
- DM74LS138 3-to-8-line decoders incorporates 3 enable inputs to simplify cascading and/or data reception
- DM74LS139 contains two fully independent 2-to-4-line decoders/demultiplexers
- Schottky clamped for high performance
- Typical propagation delay (3 levels of logic)

DM74LS138 21 ns DM74LS139 21 ns

■ Typical power dissipation

DM74LS138 32 mW

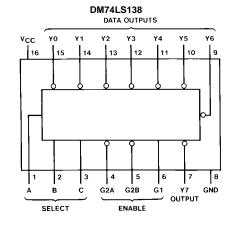
DM74LS139 34 mW

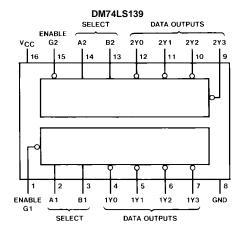
Ordering Code:

Order Number	Package Number	Package Description
DM74LS138M	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow
DM74LS138SJ	M16D	16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
DM74LS138N	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide
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Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagrams





Function Tables

DM74LS138

Inputs					Outputs							
Enable		Select			Outputs							
G1	G2 (Note 1)	С	В	Α	YO	Y1	Y2	Υ3	Y4	Y5	Y6	Y7
Х	Н	Χ	Χ	Χ	Н	Н	Н	Н	Н	Н	Н	Н
L	Χ	Χ	Χ	Χ	Н	Н	Н	Н	Н	Н	Н	Н
Н	L	L	L	L	L	Н	Н	Н	Н	Н	Н	Н
Н	L	L	L	Н	Н	L	Н	Н	Н	Н	Н	Н
Н	L	L	Н	L	Н	Н	L	Н	Н	Н	Н	Н
Н	L	L	Н	Н	Н	Н	Н	L	Н	Н	Н	Н
Н	L	Н	L	L	Н	Н	Н	Н	L	Н	Н	Н
Н	L	Н	L	Н	Н	Н	Н	Н	Н	L	Н	Н
Н	L	Н	Н	L	Н	Н	Н	Н	Н	Н	L	Н
Н	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	L

DM74LS139

	Inp	outs		Outputs						
İ	Enable Select		Outputs							
ĺ	G	В	Α	Y0	Y1	Y2	Y3			
İ	Н	Х	Χ	Н	Н	Н	Н			
	L	L	L	L	Н	Н	Н			
	L	L	Н	Н	L	Н	Н			
	L	Н	L	Н	Н	L	Н			
	L	Н	Н	Н	Н	Н	L			

H = HIGH Level

L = LOW Level X = Don't Care

Note 1: G2 = G2A + G2B

Logic Diagrams

